SERVICE MANUAL & TROUBLESHOOTING GUIDE FOR



7521 Plus/N

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7521Plus / N N/B MAINTENANCE

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1. Hardware Engineering Specification

1.1 Introduction

1.1.1 General Description

This document describes the engineering specification for 7521 plus portable notebook computer system.

1.1.2 System Overview

The 7521 plus model motherboard will accept Intel Pentium III at FSB 133/100MHz and Celeron at FSB 66MHz processor with FC-PGA packaged. Those are Pentium III 600/650/667/700/733/ 750/800/866 MHz, and Celeron 3/566/600/633/667/700/733/766 MHz.

This system is based on PCI architecture and is fully compatible with IBM PC/AT specification, which has standard hardware peripheral interface. The power management complies with Advanced Configuration and Power Interface (ACPI) 1.0. It also provides easy configuration through CMOS setup, which is built in system BIOS software and can be pop-up by pressing F2 key at system start up or warm reset. System also provides icon LEDs to display system status, such as AC Power indicator, FDD, HDD, NUM LOCK, CAP LOCK, SCROLL LOCK, SUSPEND MODE and battery present, capacity & charging status. It also equipped with LAN, FIR, USB port, 3D stereo audio and TV-OUT functions.

The memory subsystem supports 64MB on board SDRAM, one 144pin SO-DIMM socket for upgrading up to 320MB.

The SiS630S integrates the north bridge chip, super south bridge and the real 128-bit 3D graphics accelerator all into one single chip. It provides, 3D Positional Audio, Advance H/W DVD playback and 2D/3D graphics engine.

The TI 1225 cardbus controller supports PCMCIA and CARDBUS. The National Semiconductor PC97338 Super I/O controller integrates the standard PC I/O functions: floppy interface, two FIFO serial ports, one EPP/ECP capable parallel port, and support for an IrDA 1.1, 1.0 and sharp ASK compatible infrared interface. To provide for the increasing number of multimedia applications, a CODEC CS4299 is integrated onto the motherboard that support 16-bit stereo, Sound Blaster Pro, Windows Sound System compatibility, and full-duplex capabilities to meet the demands of interactive multimedia applications.

The SiS900 is a single chip 10/100Mbps Fast Ethernet LAN solution, which fully integrates both the Media Access Controller (MAC) with PCI bus master interface and 802.3u compliant 10/100Mbps physical layer interface into a 128 pins PQFP, 0.35um process chip. It is targeted at low-cost, low-power, high volume desktop PC motherboards, mobile PC module, adapter cards, and embedded systems.

The Chrontel's CH7005 digital PC to TV encoder is a standalone integrated circuit that provides a PC 99 compliant solution for TV output. It provides a universal digital input port to accept a pixel data stream from a compatible VGA controller (or equivalent) and converts this directly into NTSC or PAL TV format.

A full set of software drivers and utilities are available to allow advanced operating systems such as Windows 98 or Windows ME to take full advantage of the hardware capabilities. Features such as bus mastering IDE, Plug and Play, Advanced Power Management (APM) with application restart, software-controlled power shutdown. Following chapters will have more detail description for each individual sub-systems and functions.

1.2 Hardware System

1.2.1 System parts

Central Processing Unit : using Intel Pentium III or Celeron microprocessors in FC-PGA packaged.

Synthesizer : ICS9248-102.

SiS630S : CPU/PCI and CPU/AGP Bridge with memory controller/IDE/USB/PMU controller.

Super I/O Controller : NS PC97338VJG.

PCMCIA Interface Controlle : TI 1225.

Keyboard System : Hitachi H8 (3434F) universal keyboard controller.

3D Audio System : CRYSTAL CS4299 CODEC.

FIR port: HP HSDL-3600#007 FIR module.

FAX/MODEM : Software Modem (option).

LAN : SiS900

CH7005 : Digital PC to TV Encoder with Macrovision™

1.2.2 CPU MODULE

Intel Pentium III/Celeron Processors with 370 pins FC-PGA package.

Pentium III 600/650/667/700/733/750/800 MHz, FC-PGA package at FSB 133/100Mhz.

Celeron 600/633/667/700/733 MHz, FC-PGA package at FSB 66Mhz.

1.2.3 Synthesizer

System frequency synthesizer : ICS9248-102

Maximized EMI suppression using Integrated Circuit System spread spectrum technology.

Three copies of CPU output, output to output skew between them within 175ps and seven copies of PCI output, output to output skew within 500ps, fourteen copies of SDRAM output, output to output skew between them within 250ps.

One 48MHz output for USB and selectable 24/48MHz output (pin 25).

Two buffer copies of 14.318MHz input reference signal.

Supports up to 166MHz CPU or SDRAM operation.

Supports two SDRAM DIMMS.

Ideal for high performance Desktop/Notebook designed using SIS630 chip set.

I²C serial configuration interface.

1.2.4 SiS630S Slot 1/Socket 370 2D/3D Ultra-AGP™

Single Chipset

The single chipset, SiS630S, provides a high performance/low cost Desktop solution for the Intel Slot 1 and socket 370 series CPUs based system by integrating a high performance North Bridge, advanced hardware 2D/3D GUI engine, Super-South bridge and an AGP4X Slot. In addition, SiS630S provides system-on-chip solution that complies with Easy PC Initiative which supports Instantly Available/OnNow PC technology, USB, Legacy Removal and Slotless Design and FlexATX form factor.

By integrating the UltraAGP TM technology and advanced 64-bit graphic display interface, SiS630S delivers AGP 4x performance and memory bandwidth of up to 1 GB/s. In addition, SiS also supports an extra AGP Slot that supports 4X and Fast Write transactions. Furthermore, SiS630S provides powerful hardware decoding DVD accelerator to improve the DVD playback performance. In addition to providing the standard interface for CRT monitors, SiS630S also provides the Digital Flat Panel Port (DFP) for a standard interface between a personal computer and a digital flat panel monitor. To extend functionality and flexibility, SiS also provides the “ Video Bridge ” (SiS301) to support the NTSC/PAL Video Output, Digital LCD Monitor and Secondary CRT Monitor, which reduces the external Panel Link transmitter and TV-Out encoder for cost effected solution. SiS630S adopts Share System Memory Architecture which can flexibly utilize the frame buffer size up to 64MB.

The “ Super-South Bridge “ in SiS630S integrates all peripheral controllers/accelerators /interfaces. SiS630S provides a total communication solution including 10/100Mb Fast Ethernet for Office requirement and 1Mb HomePNA for Home Networking. SiS630S offers AC’7 compliant interface that comprises digital audio engine with 3D-hardware accelerator, on-chip sample rate converter, and professional wavetable along with separate modem DMA controller. SiS630S also provides interface to Low Pin Count (LPC) operating at 33 MHz clock which is the same as PCI clock on the host, and dual USB host controllers with six USB ports that deliver better connectivity and 2 x 12Mb bandwidth.

The built-in fast PCI IDE controller supports the ATA PIO/DMA, and the Ultra DMA33/66/100 function that supports the data transfer rate up to 100 MB/s. It provides the separate data path for two IDE channels that can eminently improve the performance under the multi-tasking environment.

SiS630S Features

Host Interface Controller

Supports Intel Slot 1/Socket370 Pentium II/!!! CPUs

Synchronous Host/DRAM Clock Scheme

Asynchronous Host/Dram Clock Scheme

Integrated DRAM Controller

3-DIMM/6-Bank of 3.3V SDRAM

Supports Memory Bus up to 133 MHz

System Memory Size up to 1.5 GB

Up to 512MB per Row

Supports 16Mb, 64Mb, 128Mb, 256Mb, 512Mb SDRAM Technology

Suspend-to-RAM (STR)

Relocatable System Management Memory Region

Programmable Buffer Strength for CS#, DQM[7:0], WE#, RAS#, CAS#, CKE, MA[14:0] and MD[63:0]

Shadow RAM Size from 640KB to 1MB in 16KB increments

Two Programmable PCI Hole Areas

Integrated A.G.P. Compliant Target /66Mhz Host-to-PCI Bridge

AGP v2.0 Compliant

Supports Graphic Window Size from 4MBytes to 256MBytes

Supports Pipelined Process in CPU-to Integrated 3D A.G.P. VGA Access

Supports 8 Way, 16 Entries Page Table Cache for GART to Enhance Integrated A.G.P. VGA Controller Read/Write Performance

Supports PCI-to-PCI Bridge Function for Memory Write from 33MHz PCI Bus to Integrated A.G.P. VGA

Supports Additional AGP slot with 4X and Fast Write Transaction

Meet PC99 Requirements

PCI 2.2 Specification Compliant

High Performance PCI Arbiter

Supports up to 4 PCI Masters

Guaranteed Minimum Access Time for CPU and PCI Masters

Integrated Host-to-PCI Bridge

Zero Wait State Burst Cycles

CPU-to-PCI Pipeline Access

256B to 4KB PCI Burst Length for PCI Masters

PCI Master Initiated Graphical Texture Write Cycles Re-mapping

Reassembles PCI Burst Data Size into Optimized Block Size

Fast PCI IDE Master/Slave Controller

Supports PCI Bus Mastering

Native Mode and Compatibility Mode

PIO Mode 0, 1, 2, 3, 4

Multiword DMA Mode 0, 1, 2

Ultra DMA 33/66/100

Two Independent IDE Channels Each with 16 DW FIFO

Virtual PCI-to-PCI Bridge

Integrated Ultra AGP VGA for Hardware 2D/3D Video/Graphics Accelerators

Supports Tightly Coupled 64 Bits Host Interface to VGA to Speed Up GUI Performance and Video Playback Frame Rate

AGP v. 2.0 Compliant

Zero-Wait-State 128x4 Post-Write Buffer with Write Combine Capability

Zero-Wait-State 128x4 2-Way Read Ahead Cache Capability

Re-locatable Memory-Mapped and I/O Address Decoding

Flexible Design Shared Frame Buffer Architecture for Display Memory

Shared System Memory Area up to 64MB

Built-in 8K Bytes Texture Cache

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32-Bit VLIW Floating-Point Primitive Setup Engine

Supports Flat and Gouraud Shading

Supports High Quality Dithering

Supports Bump Mapping

Supports Z-Test, Stencil Test, Alpha Test and Scissors Clipping Test

Supports Z Pre-Test for Reducing Texture Read DRAM Bandwidth

Supports Individual Z-Buffer and Render Buffer at the Same Time

Supports 16/24/32 BPP Z Buffer Integer/Floating Formats

Supports 16/32 BPP Render Buffer Format

Supports 1/2/4/8 Stencil Format

Supports Per-Pixel Texture/Fog Perspective Correction

Supports MIPMAP with Point-Sampled, Linear, Bi-Linear and Tri-Linear Texture Filtering

Supports Single Pass Two MIPMAP Texture, One Texture on Clock

Supports up to 2048x2048 Texture Size

Supports 2’S Power of Width and Height Structure Rectangular Texture

Supports 1/2/4/8 BPP Palletize Texture with 32 Bit ARGB Format

Supports Palette for High Performance Palette Look Up

Supports 1/2/4/8 BPP Luminance Texture

Supports 1/2/4/8 BPP Intensity Texture

Supports 8/16/24/32 BPP RGB/ARGB Texture Format

Supports Video YUV Texture in All Supported Texture Formats

Supports MIP-Mapped Texture Transparency, Blending, Wrapping, Mirror and Clamping

Supports Fogging and Alpha Blending

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Internal Full 32 Bits ARGB Format Ultra Pipelined Architecture for Ultra High Performance and High Rendering Quality

128-Bit 2D Engine with a Full Instruction Set

Built-In 64x64x2 Bit-Mapped Hardware Cursor

Built-In 32x32x16, 32x32x32 Bit-Mapped Color Hardware Cursor

Maximum 64 MB Frame Buffer with Linear Addressing

MPEG-2 ISO/IEC 13818-2 MP@ML and MPEG-1 ISO/IEC 11172-2 Standards Compliant

Supports Hardware DVD Accelerator

Direct DVD to TV Playback

Supports Single Frame Buffer Architecture

Supports Two Independent Video Windows with Overlay Function and Scaling Factors

Supports YUV-To-RGB Color Space Conversion

Supports Bi-Linear Video Interpolation with Integer Increments of Pixel Accuracy

Supports Graphic and Video Overlay Function

Supports CD/DVD to TV Playback Mode

Simultaneous Graphic and TV Video Playback Overlay

Supports Current Scan Line of Refresh Red-Back and Interrupt

Supports Tearing Free Double/Triple Buffer Flipping

Supports Input Video Vertical Blank or Line Interrupt

Supports RGB555, RGB565, YUV422 and YUV420 Video Playback Format

Supports Filtered Horizontal Up and Down Scaling Playback

Supports DVD Sub-Picture Playback Overlay

Supports DVD Playback Auto-Flipping

Built-in Two Video Playback Line Buffers

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Built-in Programmable 24-bit True-Color RAMDAC up to 270 MHz Pixel Clock RAMDAC Snoop Function

Built-in Reference Voltage Generator and Monitor Sense Circuit

Supports Down-Loadable RAMDAC for Gamma Correction in High Color and True Color Mode

Built-in Dual-Clock Generator

Supports Multiple Adapters and Multiple Monitors

Built-in PCI Multimedia Interface

Supports Digital Flat Panel Port for Digital Monitor (LCD Panel)

Built-in VESA Plug and Display for CH7003, PanelLink TM and LVDS Digital Interface

Built-in Secondary CRT Controller for Independent Secondary CRT, LCD or TV digital output

Supports VESA Standard Super High Resolution Graphic Modes

-640x480 16/256/32K/64K/16M colors 120 Hz NI

-800x600 16/256/32K/64K/16M colors 120 Hz NI

-1024x768 256/32K/64K/16M colors 120 Hz NI

-1280x1024 256/32K/64K/16M colors 85 Hz NI

-1600x1200 256/32K/64K/16M colors 85 Hz NI

-1920x1440 8bbp/16bbp 60NI

Low Resolution Modes

Supports Virtual Screen up to 4096x4096

Fully DirectX 7.0 Compliant

Efficient and Flexible Power Management with ACPI Compliance

Supports DDC1, DDC2B and DDC 3.0 Specifications

Cooperate with “ SiS Video Bridge ” to Support

-NTSC/PAL Video Output

-Digital LCD Monitor

-Secondary CRT Monitor

Low Pin Count Interface

Forwards PCI I/O and Memory Cycles into LPC bus

Translates 8/16 bit DMA cycles into PCI bus cycles

Advanced PCI H/W Audio & Modem

Advanced Power Management

Meets ACPI 1.0 Requirements

Meets APM 1.2 Requirements

ACPI Sleep States Include S1, S3, S4, S5

CPU Power States Include C0, C1, C2 C3

Power Button with Override

RTC Day-of-Month, Month-of-Year Alarm

24-bit Power Management Timer

LED Blinking in S0,S1 and S3 States

System Power-Up Events Include: Power Button, Hot-Key, Keyboard Password/ Hot Key, RTC Alarm, Modem Ring-In, SMBALY#, LAN, PME#, AC'97 Wake-Up and USB Wake-Up

Software Watchdog Timer

Power Supply'98 Support

PCI Bus Power Management Interface Spec. 1.0

Integrated DMA Controller

Two 8237A Compatible DMA Controller

8/16 bit DMA data transfer

Distributed DMA Support

Integrated Interrupt Controller

Two 8237A Compatible DMA Controller

Two 8259A Compatible Interrupt Controllers

Level or Edge Triggered programmable

Serial IRQ

Interrupt Source Re-routable to Any IRQ channel

Three 8254 Compatible Programmable 16-bits counters

System timer interrupt

Generate refresh request

Speaker output

Integrated Keyboard Controller

Hardwired Logic Provides Instant Response

Supports PS/2 Mouse Interface

Password Security and Password Power-Up

System Sleep and Power-Up by Hot-Key

KBC and PS2 Mouse Can Be Individually Disabled

Integrated Real Time Clock (RTC) with 256B CMOS SRAM

Supports ACPI Day-Month and Month-of-Year- Alarm

256 Bytes of CMOS SRAM

Provides RTC H/W Year 2000 Solution

Universal Serial Bus Host Controller

Open HCI Host Controller with Root Hub

Two USB Host Controllers

Six USB Ports

Supports Legacy Devices

Over Current Detection

I²C Bus/SMBus Series Interface

Integrated Fast Ethernet Controller and MAC Interface

Plug and Play Compatible

High-Performance 32-Bit PCI Bus Master Architecture with Integrated Direct Memory Access (DMA) Controller for Low CPU and Bus Utilization

Supports an Unlimited PCI Burst Length

Supports Big Endian and Little Endian Byte Alignments

Implements Optional PCI 3.3v Auxiliary Power Source 3.3Vaux Pin And Optional PCI

IEEE 802.3 and 802.3u Standard Compatible

Single 25MHz Clock for 10 and 100 Mbps Operation

Supports Software, Enhanced Software, and Automatic Polling Schemes to Internal PHY Status Monitor and Interrupt

Supports 10base-T, 100base-Tx 1Mb Home Networking

NAND Tree for Ball Connectivity Testing

672-Balls BGA Package

1.8V Core with Mixed 3.3V and 5V I/O CMOS Technology

1.2.5 Super IO: NS PC 97338VJG

High speed PC16550A compatible UART with receive/transmit 16 Bytes FIFO programmable serial baud rate generator

Multi-mode parallel port support including standard port, EPP/ECP (IEEE1284 compliant, 2 interrupt pins)

Plug and Play module

FDC, 100% IBM compatible, S/W & register compatible to 82077 with 16Bytes data FIFO

Support 3-Mode FDD

FIR/MIR/SIR/SHARP ASK for Infrared application.

COM2

IrDA 1.0/ IrDA 1.1/ SHARP ASK

Baud rate: max. 4Mb

Link distance: 0.01 to 1 m

Half angle : ±15°

Bit Error Rate (BER) : 10 -9

Peak wavelength : 0.85 - 0.90 μm

TQFP 100 pins

Standby mode: control by software

Default configuration :

	IO address	IRQx	DRQx
COM1	3F8-3FF	4	-
FIR/MIR/SIR/ SHARP ASK (COM2)	278-27F	3	-
PIO	378-37F	7	-
FDD	3F0-3FF	6	2

1.2.6 PC CARD interface controller : TI1225

ACPI 1.0 Compliance

PCI Power Management interface specification 1.0 Compliance

Supports distributed DMA (DDMA) and PC/PCI DMA

Advanced submicron, low-power CMOS technology.

Supports two I/O windows and two memory windows available to each cardbus socket.

Supports five PCI memory windows and two I/O windows available to each PC CARD16 socket.

Supports Burst Transfers To Maximize Data Throughput On Both PCI Buses

Provides Serial Interface To TI TPS2202/TPS2206 Dual Slot PC CARD Power Interface Switch

Supports up to 5 general purpose I/O

Multi-Function PCI Device With Separate Configuration Space For Each Socket

Pipelined architecture allows greater than 130Mbps second throughput from cardbus to PCI and from PCI to cardbus.

Support PCI Bus Lock (/LOCK)

3.3-V core logic with universal PCI interface

PCI Local Bus Specification Revision 2.1 compliant

Fully compatible with the Intel 430TX(Mobile Triton II) chipset

1995 PC Card Standard compliant

Supports two 16-bit PC card or Cardbus card; sockets powered at 3.3V or 5V with hot insertion and removal

Provides a serial EEPROM interface for loading the subsystem ID and subsystem vendor ID.

ExCA compatible registers mapped in memory or I/O space.

Supports ring indicate output, SUSPEND#, and programmable output select for CLKRUN#.

Provides socket activity LED signals.

Provides zoom video support signals.

Provides zoom video port function in socket B.

208-Pin LQFP package

1.2.7 DUAL-SLOT PC CARD POWER INTERFACE SWITCH : TPS2206

Fully Integrated VCC and V pp Switching for Dual-Slot PC Card Interface

I2C 3-Lead Serial Interface Compatible With CardBus Controllers

3.3 V Low-Voltage Mode

Meets PC Card Standards

RESET for System Initialization of PC Cards

12-V Supply Can Be Disabled Except During 12-V Flash Programming

Short Circuit and Thermal Protection

30-Pin SSOP (DB) and 32-Pin TSSOP (DAP)

Compatible With 3.3-V, 5-V and 12-V PC Cards

Break-Before-Make Switching

1.2.8 Keyboard system : H8 (3434F) universal keyboard controller

CPU

Two-way general register configuration

Eight 16-bit registers or Sixteen 8-bit registers

High-speed operation

Maximum clock rate: 16Mhz at 5V

Memory

Include 32KB ROM and 1KB RAM

16-bit free-running timer

One 16-bit free-running counter

Two output-compare lines

Four input capture lines

8-bit timer (2 channels)

Each channel has one 8-bit up-counter, two time constant registers

PWM timer (2 channels)

Resolution: 1/250

Duty cycle can be set from 0 to 100%

I^2C bus interface (one channel)

Include single master mode and slave mode

Host interface (HIF)

8-bit host interface port

Three host interrupt requests (HIRQ1, 11,12)

Regular and fast A20 gate output

Keyboard controller

Controls a matrix-scan keyboard by providing a keyboard scan function with wake-up Interrupts and sense ports

A/D converter

10-bit resolution

8 channels: single or scan mode (selectable)

D/A converter

8-bit resolution

2 channels

Interrupts

Nine external interrupt lines: NMI#, IRQ0 to 7#

26 on-chip interrupt sources

Power-down modes

Sleep mode

Software standby mode

Hardware standby mode

A single chip microcomputer

On-chip flash memory

Maximum 64-kbyte address space

Support three PS/2 port for external keyboard, mouse and internal track pad.

Support SMI, SCI trigger input:

Cover switch

Battery charging control

Smart Battery monitoring

Control D/D system on/off

Fan control and LED indicator serial interface

100pin TQFP

1.2.9 System BIOS

See software BIOS specification

1.2.9.1 System BIOS and Software Features Overview

Including System BIOS, VGA BIOS, POST, APM, PnP, ACPI and PXE BIOS

Support Shadow RAM BIOS Feature

Support APM 1.2

Support ACPI V1.0B

Support DMI 2.3

Support SMBIOS 2.2

Support Quite Boot

Support Extended Int14H function 50H (IR type switching)

Support Hot-Plug for PS/2 keyboard and pointing devices.

Support Intel CPU Microcode Update function

Support Power management S0, S1, S3, S4

Parallel Port Support- Standard / Bi-Directional / EPP(1.9) / ECP

PC99A Compliance

The following device can be disabled by BIOS

Serial Port

Parallel Port

Audio

Ethernet

Modem

(When disable the device, the resource of its device are released)

1.2.9.2 BIOS Setup Feature Introduction

Setup Utility allows you to enter the system configuration information. This information is needed by the system to identify the type of device installed and to setup special features. Typical configuration information includes the data and time, the type of disk drives, and the amount of memory; special features include Security and Power Saving.

The configuration information is stored in a special kind of memory called CMOS (Complementary Metal Oxide Semiconductor) RAM. CMOS RAM data are backed up by a RTC backup battery.

You may need to run Setup Utility when :

You see an error message on the screen requesting you to run Setup Utility.

❑ You change factory default settings for some special features.

❑ You want to modify the configuration information.

During POST, the end user can press <F2> to enter Setup and change the system parameters originally specified in the BIOS defaults. The purpose of Setup is the following:

❑ Change system hardware

❑ Change system behavior

❑ Optimize system performance

1.2.10 POWER MANAGEMENT

ACPI Introdution

The system BIOS is conform with ACPI1.0B specification.

Concept

ACPI (Advanced Configuration and Power Interface) replaces APM and PnP functionality, it's a Operating-System controlled Power Management and a subset of OnNow system.

The general behavior of a PC with OnNow is as follows:

- ❑ Minimized or eliminated Startup and shutdown delays.
- ❑ Both hardware and software can be made to trigger wake-up events.
- ❑ The PC is perceived to be off when not in use but still capable of responding to wake-up events.

ACPI Power States

- G0~G3 : Global power states
- S0~S5 : System power states
- B0~B3 : Bus power states
- C0~C3 : Processor power states
- D0~D3 : Device power states

Summary of Global Power States

Global System State	Software Runs	Latency	Power Consumption	OS restart required	Safe to disassemble computer	Exit state electronically
G0 - Working	Yes	0	Large	No	No	Yes
G1 - Sleeping	No	>0 varies with sleep state	Smaller	No	No	Yes
G2/S5-Soft off	No	Long	Very near 0	Yes	No	Yes
G3-Mechanical Off	No	Long	RTC battery	Yes	Yes	No

Summary of Device Power Sates

Device State	Power Consumption	Device Context Retained	Driver Restoration
D0 – Fully On	As needed for operation	All	None
D1	D0>D1>D2>D3	>D2	<D2
D2	D0>D1>D2>D3	<D1	>D1
D3 – Off	0	None	Full init and load

System States

1. Working (S0)

System is fully usable. User can enter working state from S4 or S5 by pressing the power button or wake up from sleeping state.

2.Sleeping State (S3)

The S3 sleeping state is a low wake-up latency sleeping state where all system context is lost except system memory. CPU, cache, and chip set context is lost in this state.

This state is attained by:

• Set " Low Battery Alarm Actions " to " Standby ", when the battery discharge to a critical level, unit will enter this state.

• If sets optional action of " cover switch ", " power button ", " sleep button " to " Standby ", and presses these buttons, or sets " System standby " timeout.

• Set " System standby " in " Power Schemes " for system inactivity time out.

• Putting the PC into standby through the Operating System by clicking Start, Shut Down then select Standby item.

Events that can bring the platform back to Working state :

•. Pressing any key on the keyboard.

•. Wake on LAN.

•. Modem answering call.

•. Pressing the power button less than 4 seconds.

3.Hibernation (S4)

The S4 sleeping state is lowest power, longest wake-up latency sleeping state supported by ACPI. The platform context is maintained. For entering this state, users have to check " Enable Hibernate " in " Power Management "of control panel.

This state is attained by:

• Set " Low Battery Alarm Actions " to " Hibernate " when the battery discharge to a critical level, unit will enter this state.

• If user sets optional action of " cover switch ", " power button ", "sleep button " to " hibernate ", and presses these buttons, the platform will enter this state.

• Set "System hibernate " in " Power Schemes " for system inactivity time out.

Events that can bring the platform back to Working state:

• Pressing the power button.

4.Soft Off State (S5)

The S5 state is similar to the S4 state except the OS does not save any context nor enable any device to wake the system. The system is in the " soft "off state and requires a complete boot when awakened.

This state is attained by:

• Shut down the PC through the Operating System by clicking Start, Shutdown, then Ok.

• Reset the PC by holding the Power button for more than 4 seconds.

Note: (1) This action may cause date loss. (2) This action normally causes the OS to run Scan Disk after reboot.

Events that can bring the platform back to Working state:

• Pressing the Power button.

5.Mechanical Off

No power supplied and consumption, achieved by unplugging the machine and removing the battery. By definition, unit will return to Soft Off (S5) by restoration of power. If previous mode was Hibernation (S4), then system returns to S4.

Component Level Power Management Matrix

Component Activity	Wake up from Standby (S3) on component activity	Wake up from Hibernation (S4) on component activity	State after time out or pressing Fn+F12 From working state	Component activity is monitored, preventing sleep timeout
Floppy Drive	N/A	N/A	Power Off	Monitored by OS
Hard Drive	N/A	N/A	Power Off	Monitored by OS
Monitor	N/A	N/A	Power Off	N/A
SiS630S Audio	N/A	N/A	Power Off	Monitored by driver
SiS630S VGA	N/A	N/A	Power Off	Monitored by driver
CD/DVD Devices	N/A	N/A	Power Off	Monitored by application
Touch Pad	Doesn't wake system	Doesn't wake system	No response	Monitored by OS
USB Device	Doesn't wake system	Doesn't wake system	Power Off	Monitored by application
SiS900 LAN	Wakes System	Doesn't wake system	Power Off	Monitored by OS
Internal Modem	Wake on incoming call if application is enabled	Doesn't wake system	Power Off	Monitored by OS
External Modem on COM port	Wake on incoming call if application is enabled	Doesn't wake system	Modem Disconnect	Monitored by driver
External PS/2	Doesn't Wakes system	Doesn't wake system	Sleep State	Monitored by OS
Keyboard				
Internal Keyboard	Any key wake up system	Doesn't wake system	N/A	N/A
RTC	Wake system	Wake system	N/A	N/A
Power Button	Wake system	Wake system	N/A	N/A
ESB Button	Wake system	Wake system	N/A	N/A
Mail Button	Wake system	Wake system	N/A	N/A

APM

Concept

This platform supports Advanced Power Management (APM1.2) developed by Microsoft and Intel. APM consists of one or more layers of software that support power management in computers with power manageable hardware.

Power State

1.Full Power

Default mode. System activity detected. This is the normal state of the system. If system power management is disabled, the system remains in this state until the power is turned off.

2. Idle

An APM driver will notify the APM BIOS about CPU usage but the APM BIOS determines the action to take. Idle is a state between full system power and standby. Enable/Disable by toggling the setting in Bios Setup Menu.

Idle Mode slows down the CPU during brief periods.

This state is attained by :

• The APM driver acknowledge APM BIOS that the system is idle. The APM BIOS issues “CPU HLT “ instruction.

Events that can bring unit back to full power state :

• CPU idle until the next system event (typically an interrupt) occurs.

3.Standby

System may not be working and in a low power state with some power saving. Most devices are in a low power mode. The CPU clock is slowed. System returns quickly to full on state. Operational parameters are retained.

This state is attained by:

• Set “Standby Timeout “ in Bios Setup Menu.

• Triggered by the timeout timer of the standby timer.

Events that can bring unit back to full power state:

• Pressing any key on the keyboard.
• Wake on LAN.
• Modem answering call.

4.Suspend

System in not working and in a low power consumption state with maximum power savings . Most power managed devices are not powered. Includes stopping the CPU clock and shutting down all peripherals. Detection restores full power state. System takes a relatively long time to return to full on mode. Operational parameters are saved to be restored later when resuming.

This state is attained by:

• Triggered by the timeout timer of the suspend timer.

• Pressing “ Fn+F12 “ hot key.

• Set “ Save To Disk Timeout ” in Bios Setup Menu.

• Allowing battery discharge to the critical level.

• Events that can bring unit back to full power state:

(1) Suspend to Ram:

• Pressing any key on the internal keyboard.

• Wake on LAN.

• Modem answering call.

• Set RTC wake up timer.

(2) Suspend to Disk:

• Press power button.

5. Off

System is not working, the power supply is off. Operational parameters are not saved. System resets and initializes when transitioning to the Full on State.

Component Level Power Management Matrix

Power Status	Idle	Standby	Suspend to Ram	Suspend to Disk
Floppy Disk	Power On	Power On	Power Off	Power Off
Hard Disk	Power On	Power On	Power Off	Power Off
CD/DVD-ROM	Power On	Power On	Power Off	Power Off
Monitor	Power On	Power Off	Power Off	Power Off
Modem	Power On	Power On	Power Off	Power Off
CPU	Low Power State	Low Power State	Power Off	Power Off
SiS630S VGA	Power On	Power On	Power Off	Power Off
SiS630S Audio	Power On	Power On	Power Off	Power Off
SiS900 LAN	Power On	Power On	Power Off	Power Off

1.2.11 Memory System

HYUNDAI SDRAM cell on board13

One chip memory size : 4Banksx1Mx16bit SDRAM.

Standard 54-pin TSOP-II package.

Power supply : 3 ±0.3V

Supports One JEDEC 144-pin SO-DIMM sockets on Mother Board for expansion

Supports 3.3V SDRAM

2 banks on one socket.

SDRAM accesses time from clock: 6ns

Memory bus bandwidth: 64 bits

7521 plus Supports 64 MB SDRAM on board and one 144-pin DIMM socket for upgrading up to 320 MB of DRAM. Here are some main memory system essential characteristics :

One chip 4Banksx1Mx16bit on board 64 MB

144-pin SO-DIMM socket 1

Memory Voltage 3.3V ± 10%

Banks on DIMM Mixed type DRAM Only supports SDRAM

1.2.12 Interface

Power Supply Jack.

One Standard Parallel Port With ECP/EPP Functions

Supports Two USB port for all USB devices.

Supports Macrovision's TV-OUT connector.

Tunable volume by variable resistor.

Two Serial Ports, One For COM1/COM2, The Other For FIR/MIR/SIR/SHARP ASK.

One External CRT Connector For CRT Display.

One PS/2 Interface For External KB, Mouse Or Other Devices.

Two Cardbus Sockets.

Cable For Connection Between M/B And Panel.

Cable For Connection Between M/B And Backlight BD.

Digital (Optical, 48KHz) / Analog Line-out Jack, Line-In Jack and Microphone Input Jack.

One MODEM RJ-11 phone jack for PSTN line and RJ-45 for LAN.

Battery translation board connection between M/B and battery.

Easy start buttons translation board (ESB) connection between M/B and five Buttons.

Internet quick start button translation board (IQSB) connection between M/B and touch pad, three LEDs, Mail Received Button Buttons.

FDD-HDD translation board connection between M/B and floppy, hard disk.

One CD-ROM connector on M/B.

1.2.13 Audio System: AC'97 CODEC CS4299

AC'97 CODEC CS4299 provides a complete high quality audio solution, Feature Include :

MPU-401 interface

FM synthesizer

Game Port

MIDI port.

MODEM

CD-ROM

Volume Control: Rotary VR

Stereo BTL 2x1 W amplifiers (TPA0202) with 8-Ohm Load.

CD-ROM IDE interface.

18-bit stereo ADC & 20-bit stereo DAC for record and play back.

Programmable sample rates from 20Hz to 20kHz for record and playback.

Digital (optical, 48KHz)/ analog line-out port * 1 (3.5 mm phone-jack and SCMS support)

Line-in * 1(3.5 mm phone-jack)

Built-in speaker * 2 (1w, 8 ohm)

Built-in microphone * 1

Note: for those input source not using should be set mute in order to reduce noise.

1.2.14 IR MODULE: HSDL-3600#007

Fully Compliant to IrDA 1.1 Specifications
- 115.2 kb/s to 4 Mb/s operation
- Excellent nose-to-nose operation

Compatible with ASK, HP-SIR, and TV Remote

IEC825-Class 1 Eye Safe

Wide Operating Voltage Range
- 2.7 V to 5.25 V

Small Module Size
- 4.0 x 12.2 x 5.1 mm (HxWxD)

Complete Shutdown
- TXD, RXD, PIN diode

Low Shutdown Current
- 10 nA typical

Adjustable Optical Power Management
- Adjustable LED drive-current to maintain link integrity

Single Rx Data Output
- FIR Select pin switch to FIR

Integrated EMI Shield
- Excellent noise immunity

Edge Detection Input
- Prevents the LED from long turn-on time

Interface to various Super I/O and Controller Devices

Designed to Accommodate Light Loss with Cosmetic Window

Minimum External Components Required

1.2.15 SiS900 Fast Ethernet PCI Bus 10/100Mbps LAN Single Chip with OnNow Support

SiS900 is a single chip 10/100Mbps Fast Ethernet LAN solution, which fully integrates both the Media Access Controller (MAC) with PCI bus master interface and 802.3u compliant 10/100Mbps physical layer interface into a 128 pins PQFP, 0.35um process chip. It is targeted at low-cost, low-power, high volume desktop PC motherboards, mobile PC module, adapter cards, and embedded systems.

SiS900 fully implements the PCI bus version 2.1 interface for host communications. Packet descriptors and data are transferred via bus-mastering DMA channels, reducing the burden on the host CPU. The buffer management scheme utilized by SiS900 optimizes the use of memory space and the system bus. Descriptor information, describing the buffer space in which packet information is held, is symmetrical between transmit and receive operations. SiS900 supports both half-duplex and full-duplex operations with minimum inter frame gap and IEEE802.3x full-duplex flow control. In order to meet the PC 98 and the Green PC power saving requirements, SiS900 supports ACPI and Network Device Class Power Management specification. All the device states of D0, D1, D2, D3hot, and D3cold are implemented. SiS900 also supports Remote Wake On LAN and OnNow for the Desktop PC management. Additional features include a serial EEPROM interface for device information access and a Boot ROM interface up to 128K bytes for remote boot functions support.

SiS900 also integrates analog interface for twisted pair Fast Ethernet applications. SiS900 can be configured for either 100 Mbps (100Base-TX) or 10 Mbps (10Base-T) Ethernet operation. SiS900 consists of 4B5B/Manchester encoder/decoder, scrambler/descrambler, 100Base-TX/10Base-T twisted pair transmitter with wave shaping and output driver, 100Base-TX/10Base-T twisted pair receiver with on chip equalizer and baseline wander correction, clock and data recovery, and Auto Negotiation capability. The addition of internal output wave shaping circuitry and on-chip filters eliminates the need for external filters normally required in 100Base-TX and 10Base-T applications. SiS900 can automatically configure itself for 100 or 10 Mbps and Full or Half Duplex operation with the on-chip Auto Negotiation algorithm. SiS900 PHY can access eleven 16-bit registers through the internal Management Interface (MI) serial port. These registers contain configuration inputs, status outputs, and device capabilities.

SiS900 Features

Integrated Fast Ethernet controller and 10/100 megabit per second (Mbps) Physical Layer Transceivers for the PCI local bus

PCI specification revision 2.1 compliant

32-bit glueless PCI host interface

Plug and Play compatible

Supports PCI clock frequency from DC to 33 MHz independent of network clock

Supports network operation with PCI clock from 25Mhz to 33Mhz

Supports both +3.3v and +5v PCI signaling

High-performance 32-bit PCI bus master architecture with integrated Direct Memory

Access (DMA) Controller for low CPU and bus utilization

Supports an unlimited PCI burst length

Supports big endian and little endian byte alignments

Supports PCI Device ID, Vendor ID/Subsystem ID, Subsystem Vendor ID programming through the EEPROM interface

Implements optional PCI 3.3v auxiliary power source 3.3Vaux pin and optional PCI power management event (PME#) pin

IEEE 802.3 and 802.3u standard compatible

IEEE 802.3u Auto Negotiation and Parallel detection for automatic speed selection

Full duplex and half duplex mode for both 10 and 100 Mbps.

Fully compliant ANSI X3.263 TP-PMD physical sub-layer which includes adaptive equalization and Baseline Wander compensation.

Automatic Jam and IEEE 802.3x Auto-Negotiation for flow control

Single access to complete PHY register set

Built-in waveform shaping requires no external filters

Single 25Mhz clock for 10 and 100 Mbps operation.

Power down of 10Base-T/100Base-TX sections when not in use

Jabber control and auto-polarity correction for 10Base-T.

User programmable LED function mapping

Supports software, enhanced software, and automatic polling schemes to internal PHY status monitor and interrupt

Supports 10BASE-T, 100BASE-TX, and any future

Supports PC97, PC98, and Net PC requirements - Green PC compatible

Supports Advanced Configuration and Power Interface Specification (ACPI) Revision 1.0

Supports PCI Bus Power Management Interface Specification Version 1.0a

Supports Network Device Class Power Management Specification Version 1.0a

Supports PCI Hot-Plug Specification Revision 1.0

Implements full OnNow features including pattern matching and link status wake-up with automatic internal PHY status polling

Implements optional Magic Packet TM remote wake-up scheme

Implements IEEE 802.3x compliant Flow Control

Additional features

Internal 128-bit Multicast Hash Table address filter

Serial EEPROM support

Boot ROM supports up to 128 Kbytes

Extensive programmable internal/external loop back capabilities

+3.3V power supply with +5V tolerant I/Os

128pin PQFP package. Low-Power CMOS 0.35um Technology

1.2.16 CH7005C Digital PC to TV Encoder

The Chrontel's CH7005 digital PC to TV encoder is a standalone integrated circuit which provides a PC 99 compliant solution for TV output. It provides a universal digital input port to accept a pixel data stream from a compatible VGA controller (or equivalent) and converts this directly into NTSC or PAL TV format.

This circuit integrates a digital NTSC/PAL encoder with 9-bit DAC interface, and new adaptive flicker filter, and high accuracy low-jitter phase locked loop to create outstanding quality video. Through its TrueScale TM scaling and deflickering engine, the CH7005 supports full vertical and horizontal underscan capability and operates in 5 different resolutions including 640x480 and 800x600.

A new universal digital interface along with full programmability make the CH7005 ideal for system-level PC solutions. All features are software programmable through a standard I 2 C port, to enable a complete PC solution using a TV as the primary display.

CH7005 Features

Supports MacrovisionTM 7.X anti-copy protection

Function compatible with CH7004

Universal digital interface accepts YCrCb (CCIR601or 656) or RGB (15,16 or 24-bit) video data in both non-interlaced and interlaced formats

TrueScaleTM rendering engine supports undescam operations for various graphic resolutions

Enhanced text sharpness and adaptive flicker removal with up to 5-lines of filtering

Enhanced dot crawl control and area reduction

Fully programmable through I2C port

Supports NTSC, NTSC-EIA (Japan), and PAL (B, D, G, H, I, M and N) TV formats

Provides Composite, S-Video and SCART outputs

Auto-detection of TV presence

Supports VBI pass-through

Programmable power management

9-bit video DAC outputs

Complete Windows and DOS driver software

Offered in 44-pin PLCC, 44-pin TQFP

1.3 Special Feature Function

1.3.1 Hot Key Function

Keys Combination	Feature	Meaning
Fn + F5	LCD/external CRT switching	Rotate display mode in LCD only, CRT only and simultaneously display.
Fn + F6	Brightness down	Decreases the LCD brightness / No function in DSTN model
Fn + F7	Brightness up	Increases the LCD brightness / No function in DSTN model
Fn + F10	Enable/Disable Battery Warning Beep	Toggle Battery Warning on/off
Fn + F11	Panel Off/On	Toggle Panel Off/On
Fn + F12	Suspend to RAM/HDD	Force the computer into either Suspend to HDD or Suspend to RAM mode depending on BIOS Setup.

1.3.2 Easy Start Button function

Keys	Feature	Meaning
IQSB	Mail Received Button (or function "Recognizable Signal")	Determined by Software component.
ESB1	Entertainment Quick Key	Determined by Software component.
ESB2	Instant Internet	Determined by Software component.
ESB3	My Presario	Determined by Software component.
ESB4	Search	Determined by Software component.
ESB5	Email	Determined by Software component.

1.3.3 Flash ROM (BIOS)

7521 plus system utilizes the state-of-the-art Flash EEPROM technology. User can upgrade the system BIOS in the future just running the program from MiTAC.

1.3.4 LED Indicators

System has ten status LED indicators to display system activity which include above keyboard and below touch pad:

(1) Four LEDs indicators below touch pad :

From left to right that indicates Mail Received status, AC POWER, BATTERY POWER and BATTERY STATUS:

- MAIL RECEIVED STATUS : This LED lights to indicate that User received E-mail status. User can define color of LED (yellow or green) to indicate relation of transmitter.
- AC POWER : This LED lights green when the notebook is being powered by AC, and flash (on 1 second, off 1 second) when Suspend to DRAM is active using AC power. The LED is off when the notebook is off or powered by batteries, or when Suspend to Disk.
- BATTERY POWER : This LED lights green when the notebook is being powered by batteries, and flashes (on 1 second, off 1 second) when Suspend to DRAM is active using battery power. The LED is off when the notebook is off or powered by AC, or when Suspend to Disk.
- BATTERY STATUS : During normal operation, this LED stays off as long as the battery is charged. When the battery charge drops to 10% of capacity, the LED lights red, flashes per 1 second and beeps per 2 second. When AC is connected, this indicator glows green if the battery pack is fully charged, or orange (amber) if the battery is being charged.

(2) Six LED indicators above keyboard :

From left to right that indicates CD-ROM DRIVE, HARD DISK DRIVE, FLOPPY DISK DRIVE, NUM LOCK, CAPS LOCK and SCROLL LOCK.

1.3.5 COM port assignment

❑ COM1 : MODEM / RS-232 / Disable

❑ COM2 : IR / RS-232 / Disable

1.4 SMM and System BIOS

System Management Mode

7521 plus system has built in several power saving modes to prolong the battery usage for mobile purpose. User can enable and configure different degrees of power management modes via ROM CMOS setup (booting by pressing F2 key). Following are the descriptions of the SMM and power management modes supported.

Full On Mode

In this mode, each device is running with the maximal speed. CPU clock is up to its maximum.

Doze Mode

In this mode, CPU will be toggling between on & stop grant mode either. The technology is clock throttling. This can save battery power without loosing much computing capability. The CPU power consumption and temperature is lowered in this mode.

Standby

For more power saving, it turns off the peripheral component. In this mode, the following is the status of each device.

- CPU: Stop grant
- LCD: backlight off
- HDD: spin down
- FDD: standby

Suspend Mode

The most chipset of the system is entering power down mode for more power saving. In this mode, the following is the status of each device.

Suspend to DRAM:

- CPU : off
- SiS630 : Partial off
- VGA : Suspend
- PCMCIA : Suspend
- Super IO : off
- Audio : off
- SDRAM: Self Refresh.

Suspend to HDD:

- All devices are stopped clock and power-down,
- System status is saved in HDD.
- All system status will be restored when powered on again.

Other power management functions

HDD & Video access

System has the ability to monitor video and hard disk activity. User can enable monitoring function for video and/or hard disk individually. When there is no video and/or hard disk activity, system will enter next PMU state depending on the application. When the VGA activity monitoring is enabled, the performance of the system will have some impact.

Battery Warning

System also provides Battery capacity monitoring and gives user a warning so that users have chance to save his data before battery dead. Also, this function protects system from mal-function while battery capacity is low.

- Battery Warning: Capacity below 10%, Battery Capacity LED flashes per second, system beeps per 2 seconds. (System beeps only if BIOS setup enable Battery Warning Beeping.) System will suspend to HDD after 2 Minute if BIOS setup enable this function or system will runs until battery dead without any protection.

Cover Switch

System automatically provides power saving on monitoring Cover Switch. It will save battery power and prolong the usage time when user closes the notebook cover unintentionally but the system still in power on mode. There are two functions to be chosen.

1. Switch to CRT

2. Panel Off

3. Suspend to DRAM or Suspend to Disk by CMOS setup

Battery Warning State

7521 plus system provides battery management function and gives warning while battery is in its low power state. When the battery capacity is below 10% (Battery Warning State), system will generate beep for every 2 seconds. When hearing the beeping, it is recommended that user should plug in AC adapter to get power from external source, or stop working and save his data file to prevent disaster results.

Battery Low State

After Battery Warning State, and battery capacity is below 4%, system will generate beep for twice second.

Battery Dead State

When the battery voltage level reaches 9 volts, system will shut down automatically in order to extend the battery packs' life.

Fan power on/off management

FAN is controlled by H8 embedded controller which using LM45 to sense CPU temperature and PWM to control fan speed.

1.5 Peripheral Components

LCD Panel

- Hyundai 14X13

  1024X768 XGA TFT Panel

  Display size (diagonal): 14.1 inch

  262,144 colors display

  1 channel LVDS Interface (Flat Link, Ti)

  Display Mode: Normal White

  Back-light unit: CCFL, 1 tube

  DC for Panel: 3.3V+-0.3V

  Pixel pitch: 0.279(H) X0.279 (V)

  Power supply current: 320 mA (Typ)

  Lamp start Voltage : 1500Vrms (25 ℃)

Hard Disk Drive

- FUJITSU MHK2120AT: 12 GB Capacity

  12.0GB Capacity

  Number of head: 3

  Number of cylinders: 14,784

  Bytes per sector: 512

  Recording method: 16/17 MTR

  Track density: 24,300 TPI

  Bit Density: 383 Kbpi

Rotational Speed: 4,200 rpm +-1%

Average Latency: 7.14 ms

Interface: ATA-5 (Max. Cable length: 0.46 m)

Data transfer rate:

To/From Media: 12.5 to 22.3 MB/s

To/From Host: 66.6 MB/s Max (Ultra-DMA mode 4)

Data Buffer Size: 512 KB

Spin up current: 0.9Arms

Max. Power Consumption: 4.5W (During spin up)

Physical Dimensions (H X W X D): 9.5 mm X 100.0 mm X 70.0 mm

15GB, 20GB, 24GB HDD To Be Defined.

Keyboard

- External keyboard: Supports IBM 106 key compatible keyboard
  Key pitch: 19 mm
  Windows95 applied
- Internal keyboard: Compatible Japanese keyboard layout (90 keys)

Floppy Disk Drive

- Mitsumi D353G
- Using High density (2HD) 3.5 inch disk
- Data transfer rate: 500k bits/sec
- Disk rotational speed: 300 rpm for 2mode, 360rpm for 3mode
- Track density: 135 tip
- Track to Track time: 3msec

Touch Pad

- ❑ Logic Tech: 904255-0002
- ❑ Vcc: 5V +- 0.5
- ❑ Icc (max): 15 mA
- ❑ Interface: PS/2
- ❑ X/Y position resolution: 480+-50 CPI
- ❑ Dimension: 66mm x 50mm x 5.0mm
- ❑ Effective area: 55mm x 39 mm
- ❑ Operating Temp. : 0 - 50 degree C
- ❑ Storage humidity: 5 - 90 %,
- ❑ Storage Temp.: -20 - + 60 degree C
- ❑ ESD: 15KV applied to front surface

24X CD-ROM Drive

- ❑ System has optional MATSUSHITA UJDA150 24X speed CD-ROM drive, LGS CRN8241B 24X speed CD-ROM drive, or TEAC CD-224E-A92 24X speed CD-ROM drive.
- ❑ Hardware interface is compliant with ATAPI IDE specification.
- ❑ IDE second channel (170h). The default drive is D. User should install the CD-ROM device driver in order to operate this device. This CD-ROM drive also support audio interface. Co-operate with audio circuit, CD-ROM drive can work as a CD player.
- ❑ Ejection: Manual eject using the eject button/Automatically eject using the tray

- XM-1802B:

  Average data transfer rate of 3,600 KB/s
  Average random seek time of 100ms
  Random access time of 110ms.
  Small size (only 12.7(H) x 128(W) x 129(D) mm)
  Extremely low weight of 230g
  Low average power consumption of 2.4W (maximum only 3.2W).

DVD-ROM drive

- MATSUSHITA: UJDA520L-SH 4X speed

  Fast 170 ms Random Access Time (DVD)
  Max. 4X (DVD)/Max. 24X (CD)
  Max. 5,408 Kbytes/s (DVD)/Max. 3,600 Kbytes/s (CD) Sustained Transfer Rate.
  PIO mode-4 ATAPI Drive (16.7 Mbytes/s)
  DMA: Multi word DMA transfer mode-2 (Transfer Rate 16.7 Mbytes/s)
  Ultra DMA mode-2 (Transfer Rate 33.3 Mbytes/s)

CD-R/RW drive

- MATSUSHITA: UJDA310

  WRITE 4X-Speed
  READ max 20X-Speed (CD-RW max 14X-Speed)
  PIOMODE: 16.6MB/s; Mode 4
  DMAMODE: 4.2MB/s; Mode 0
  Write: 150KB/s (Normal speed), 300KB/s (2X speed), 600KB/s (4X speed)
  Buffer memory: 2MB
  Access speed 150ms (Typ.)

7521Plus / N N/B MAINTENANCE

LED Indicators

- ❑ Lower ICON LEDs on M/B
  - Mail Received status (left 1)
  - AC POWER (left2)
  - BATTERY POWER (right 2)
  - BATTERY STATUS (right 1)
- ❑ Upper ICON LEDs on M/B
  - CD-ROM/MO (left 1)
  - HARD DISK DRIVE (left 2)
  - FLOPPY DISK DRIVE (left 3)
  - NUM LOCK (right 3)
  - CAPS LOCK (right 2)
  - SCROLL LOCK (right 1)

IO port

- ❑ HP HSDL-3600#007 FIR Module
  - Meet IrDA Physical Layer Specification
  - 1 cm to 1 Meter Operating Distance
  - 30 degree Viewing Angle
  - Support Two Channels - 2.4 Kb/s to 115.2Kb/s and 1.15Mb/s to 4.0 Mb/s

CMOS Battery

- ❑ CR2032 3V 220mAh lithium battery
- ❑ When AC in or system main battery in, CMOS battery will no power consumption.
- ❑ AC or main battery not exists, CMOS battery life at less (220mAh/5.8uA) 4 years.
- ❑ In normal condition, battery life is at less over 4 years. Battery was put in battery holder.

Serial Interface

- ❑ Using ADM3311ARU chip
- ❑ ESD rating: ±3KV
- ❑ Lead TEMP. (Soldering 10sec): +300 ℃
- ❑ Number of RS-232 drivers: 3
- ❑ Number of RS-232 receivers: 5
- ❑ 28 pin SSOP package
- ❑ Support shutdown mode (pin 23).
- ❑ -40 ℃ - +85 ℃ operating TEMP. range
- ❑ Operating voltage range : 3V ±0.3V
- ❑ MAX. data rate: 460 kbps
- ❑ Shutdown supply current: 15(TYP) uA- 50(MAX) uA

PCMCIA Socket

- ❑Operating temperature range: -55 ℃- +85 ℃
- ❑ Insertion force: 39.2N (MAX)
- ❑ 10000 times insertion and withdrawal at the cycle rate 400- 600cycles/hour and no
- ❑ evidence of breakage and cracks on the component.
- ❑ In +85 ℃ 250h life test conditions should be no evidence of breakage and
- ❑ Cracks on the component.
- ❑ In -55 ℃ 96h life test conditions should be no evidence of breakage and
- ❑ Cracks on the component.

FAN

- ❑ Dimension: (25mmx25mmx10mm)±0.5mm
- ❑ Made by Sunonwealth Electric Machine Industry Co. Ltd.
- ❑ Model number: KD0502PEB2-8 DC brushless fan
- ❑ Operating speed: 8000 rpm.
- ❑ Input voltage: 5V
- ❑ Operating temperature: -10 - +70 degree C.
- ❑ Weight: 7g
- ❑ Direction of rotation: C.C.W.
- ❑ Noise level: 27 dB (A)
- ❑ Rated power: 0.6 W
- ❑ Static pressure: 0.09 inch-H2O
- ❑ Air delivery: 2.3 CFM

1.6 Appendix 1: GPIO definitions

GPI DEFINITIONS

Signal Name	Function	Description	During PCIRST#	After PCIRST#	S1	S3	S4/S5	Remark
GPIO [0]	Panel ID switch1	Panel ID select	In	In	Defined	Off	Off	
GPIO [1]	Panel ID switch2	Panel ID select	In	In	Defined	Off	Off	
GPIO [2]	Panel ID switch3	Panel ID select	In	In	Defined	Off	Off	
GPIO [3]	Panel ID switch4	Panel ID select	In	In	Defined	Off	Off	
GPIO [4]	KBD_US/JP#		In	In	Defined	Off	Off	
GPIO [5]	Rst_CDROM	Reset CD-ROM function	Out	Out	Defined	Off	Off	
GPIO [6]	EXTSMI#		In	In	Defined	Off	Off	
GPIO [7]	SPDIF	SPDIF output	Out	Out	Defined	Off	Off	
GPIO [8]	TV_Rset	7005 function	Out	Out	Defined	Off	Off	
GPIO [9]	CRT_isolate#		Out	Out	Defined	Off	Off	
GPIO [10]	FDD_MODE		In	In	Defined	Off	Off	
GPIO [11]	SPK_OFF#		Out	Out	Defined	Off	Off	
GPIO [12]	RS232_OFF#		Out	Out	Defined	Off	Off	
GPIO [13]	CARD_IN#		In	In	Defined	Off	Off	
GPIO [14]	CRT_IN#		In	In	Defined	Off	Off	
GPIO [15]	CARD_ACT		In	In	Defined	Off	Off	

Note 1. LCD ID

LCD_SW4	LCD_SW3	LCD_SW2	LCD_SW1	Vendor	PANEL	Description
0	0	0	0	HannStar	HSD141PX11	14.1”
0	0	0	1	Unipac	UP141X01-2	14.1”
0	0	1	0	Hyundai	14X13-101	14.1”
1	0	0	0	Hyundai	HT15X31	15”
1	0	0	1	Hitachi	TX38D85VC1CAA	15”

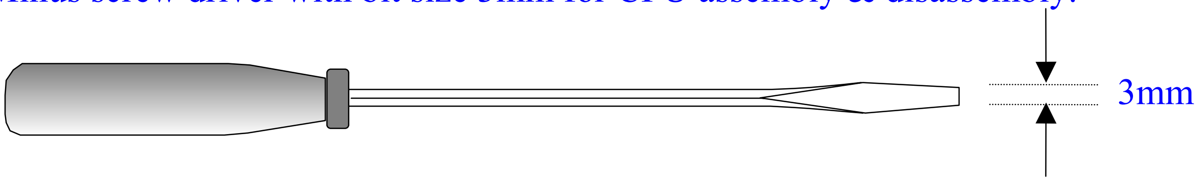
Note 3. CPU & SDRAM Frequency setting table:

SW_FS3	SW_FS2	SW_FS1	SW_FS0	CPU	SDRAM
0	0	0	0	66	100
0	0	0	1	100	100
0	0	1	1	133	100
0	1	0	0	66	133
0	1	0	1	100	133
0	1	1	1	133	133
1	0	0	0	66	66

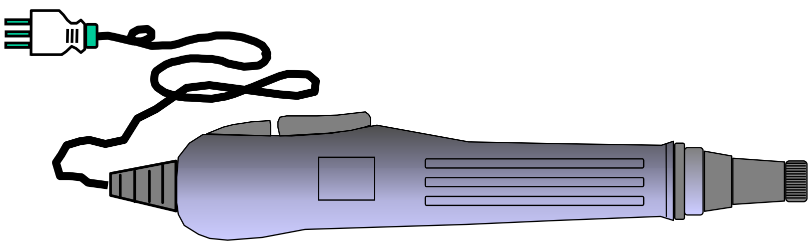
2 System View and Disassembly

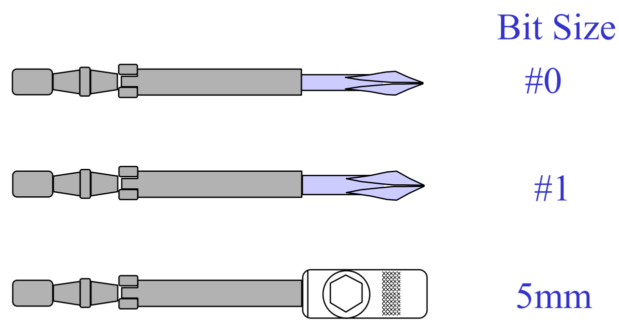
2.0 Tools introduction

1.Minus screw driver with bit size 3mm for CPU assembly & disassembly.



2. Auto screw driver for system assembly & disassembly.





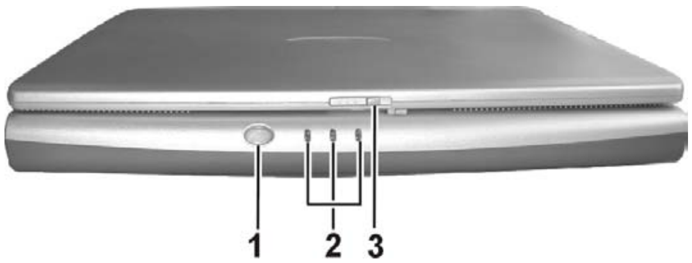
Screw Size	Tooling	Tor.	Bit Size
1. M2.0	Auto-Screw driver	2.5-3.0 kg/cm2	#0
2. M2.6	Auto-Screw driver	3.0-3.5kg/cm2	#1
3. M3.0	Auto-Screw driver	3.0-3.5kg/cm2	#1
4. Standoff 4mm	Auto-Screw driver	2.5-3.0 kg/cm2	# 5mm

2 System View and Disassembly

2.1 System View

2.1.1 Front View

❶ Mail-Received Button/Indicator
❷ Power Indicators
❸ Top Cover Latch



2.1.2 Left-Side View

❶ Audio Input Connector
❷ Microphone Connector
❸ Audio Output Connector
❹ Volume Control
❺ PC Card Slots
❻ Floppy Disk Drive

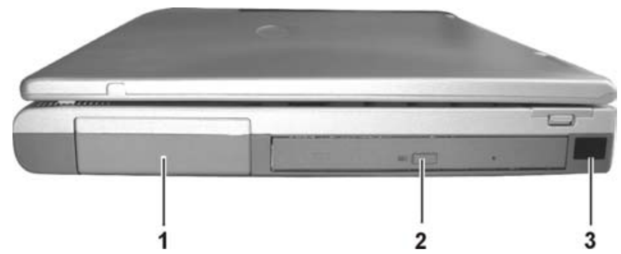


2.1.3 Right-Side View

❶ Battery Pack

❷ CD-ROM/DVD-ROM Drive

❸ IR Port



2.1.4 Rear View

❶ Power Connector

❷ PS/2 Port

❸ USB Ports

❹ Parallel Port

❺ Serial Port

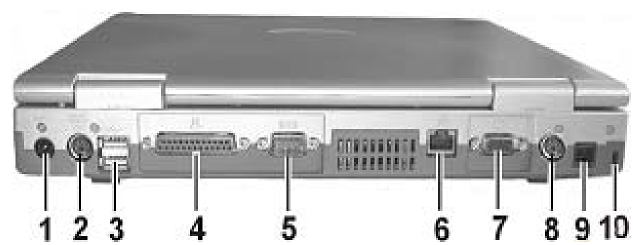
❻ RJ-45 Connector

❼ VGA Port

❽ TV-Out Connector

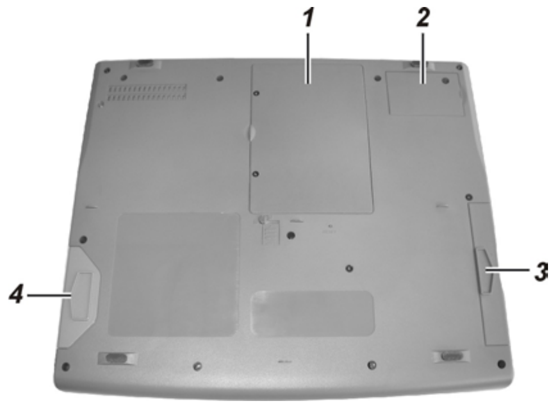
❾ RJ-11 Connector

❿ Kensington Lock



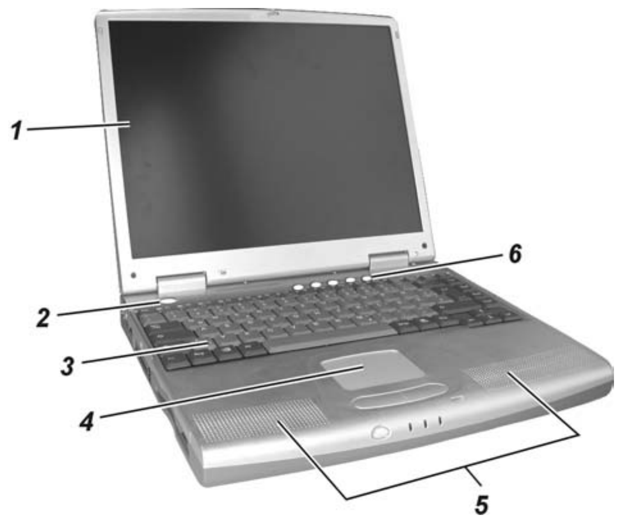
2.1.5 Bottom View

❶ CPU Cover
❷ Modem Card Cover
❸ FDD/HDD Module
❹ Battery Pack



2.1.6 Top-Open View

❶ LCD Screen
❷ Power Button
❸ Keyboard
❹ Touchpad
❺ Stereo Speaker Set
❻ Easy Start Buttons



2.2 System Disassembly

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations. Use the chart below to determine the disassembly sequence for removing components from the notebook.

NOTE: *Before you start to install/replace these modules, disconnect all peripheral devices and make sure the notebook is not turned on or connected to AC power.*

- **NOTEBOOK**
  - **Modular Components**
    - **2.2.1 Battery Pack**
    - **2.2.2 CPU**
    - **2.2.3 Modem Card**
    - **2.2.4 FDD/HDD Module**
    - **2.2.5 CD-ROM Drive**
    - **2.2.6 Keyboard**
    - **2.2.7 SO-DIMM**
  - **LCD Assembly Components**
    - **2.2.8 LCD Assembly**
    - **2.2.9 LCD Panel**
    - **2.2.10 Inverter Board**
  - **Base Unit Components**
    - **2.2.11 System Board**
    - **2.2.12 Touchpad**

2.2.1 Battery Pack

Disassembly

1. Carefully put the notebook upside down.
2. Turn the locking button to the "unlock" ( ) position (❶), then slide and hold the latch in the unlock position and pull the battery pack out of the compartment (❷).(figure 2-1)

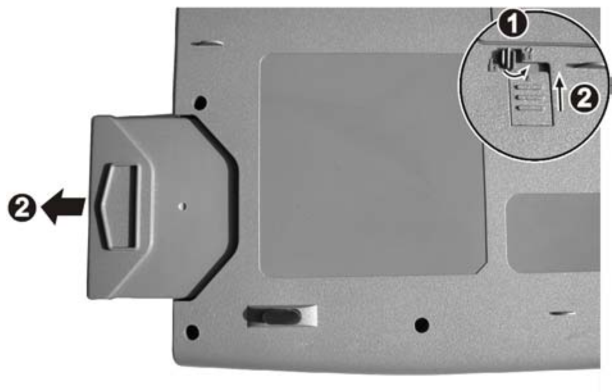


Figure 2-1

Reassembly

1. Push the battery pack into the compartment. The battery pack should be correctly connected when you hear a clicking sound.
2. Turn the locking button to the "lock" ( ) position.

2.2.2 CPU

Disassembly

1. Carefully put the notebook upside down.
2. Remove two screws locking the CPU compartment cover, and then lift the cover up. (figure 2-2)

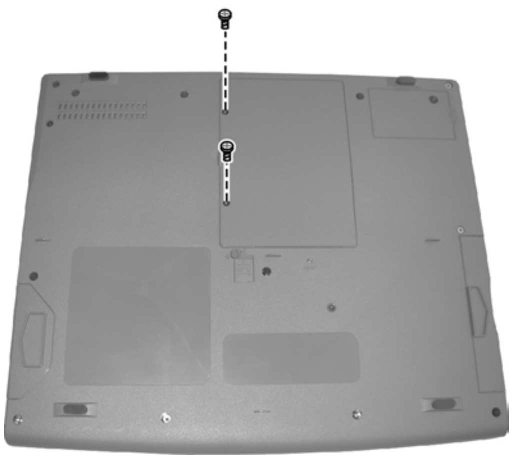


Figure 2-2

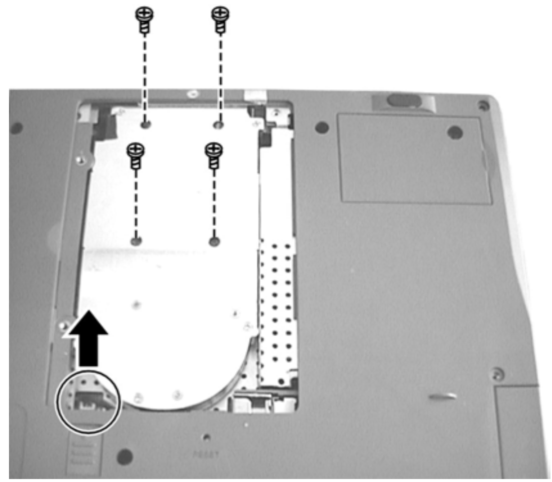


Figure 2-3

3. Remove four screws fastening the heatsink and disconnect the fan's power cord to free the heatsink from the CPU module. (figure 2-3)

4. Insert a minus screwdriver 101 (JIS standard) into the “OPEN” hole of the socket, and push the screwdriver toward the CPU to free the CPU. Now you can take out the CPU from the socket. (figure 2-4)

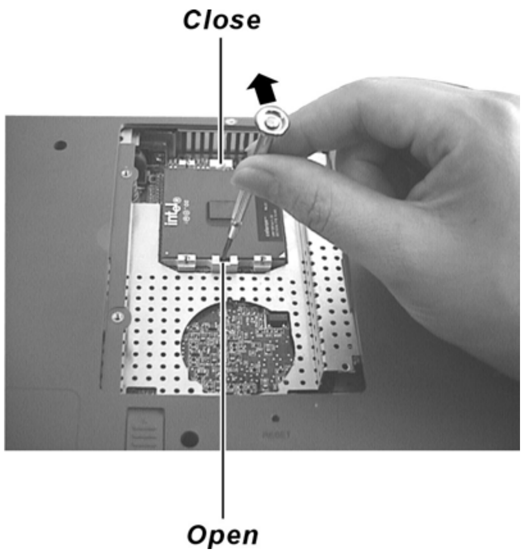


Figure 2-4

Reassembly

1. Align the arrowhead corner of the CPU with the beveled corner of the socket, and insert the CPU pins into the holes. Insert the flat screwdriver into the “CLOSE” hole of the socket, and push the screwdriver toward the CPU to secure the CPU in place.
2. Connect the fan’s power cord to the system board, fit the heatsink onto the top of the CPU and secure with four screws.
3. Replace the CPU compartment cover and secure with two screws.

2.2.3 Modem Card

Disassembly

1. Carefully put the notebook upside down.

2. Remove one screw locking the modem card compartment cover, and then lift the cover up. (figure 2-5)



Figure 2-5

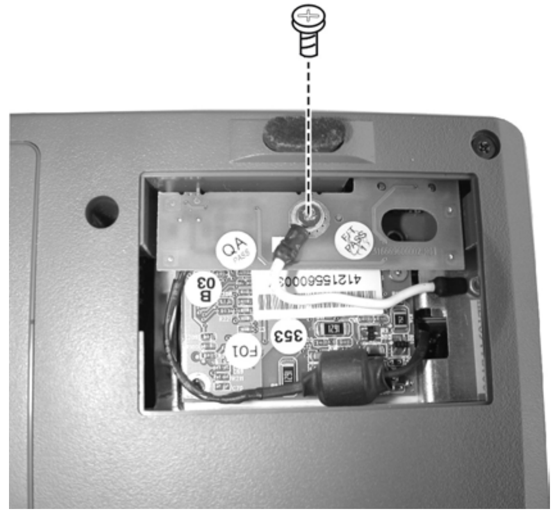


Figure 2-6

3. Remove one screw fastening the connector board and the grounding cable. (figure 2-6)

4. Slightly lift up the connector board, and then remove one screw fastening the modem card.
   Now you can take out the modem card from the compartment. (figure 2-7)

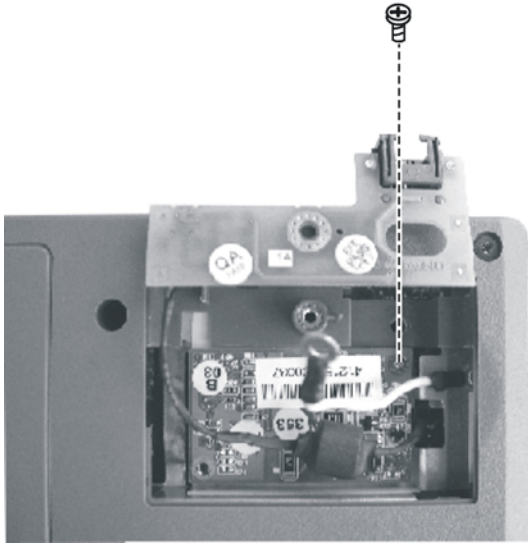


Figure 2-7

Reassembly

1. Reconnect the modem card into the system board and secure with two screws.
2. Hold the connector board an angle so that the phone line connector is pointed towards the opening on the notebook. Insert the connector into the opening and secure with a screw which fastening both the connector board and the grounding cable.
3. Replace the compartment cover and secure with one screw.

2.2.4 FDD/HDD Module

Disassembly

1. Carefully put the notebook upside down.
2. Remove one screw and slide the FDD/HDD module out of the compartment. (figure 2-8)

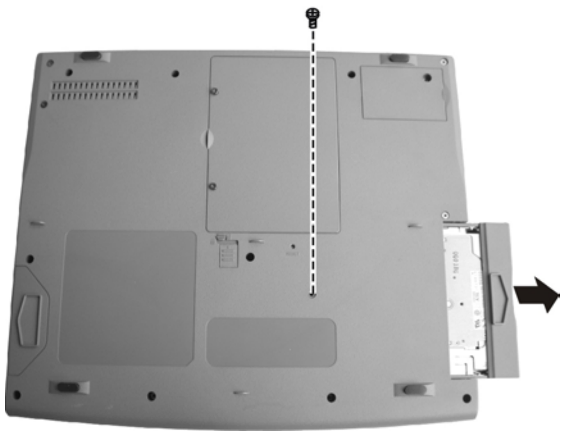


Figure 2-8

3. To take the hard disk drive apart, remove two screws of the hard disk. Then lift the hard disk up and unplug the connector to remove it. (figure 2-9)



Figure 2-9

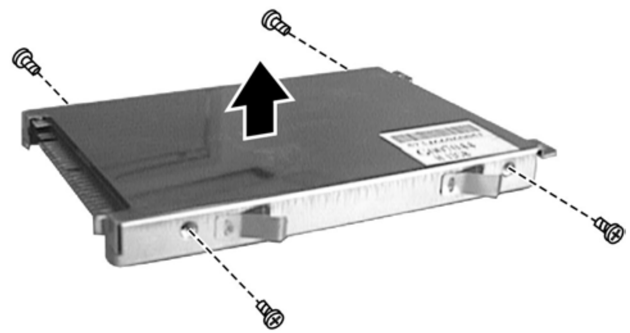


Figure 2-10

4. Remove four screws to separate the hard disk drive from the metal shield. (figure 2-10)

Reassembly

1. To install the hard disk drive, place it in the bracket and secure with four screws.
2. Connect the hard disk to the connector on the FDD/HDD module and secure with two screws.
3. Slide the FDD/HDD module into the compartment and secure with one screw.

2.2.5 CD-ROM Drive

Disassembly

1. Carefully put the notebook upside down.
2. Remove the battery pack. (See section 2.2.1 Disassembly.)
3. Remove the modem card. (See section 2.2.3 Disassembly.)
4. Remove the FDD/HDD module. (See step 2 in section 2.2.4 Disassembly.)
5. Remove one screw locking the CD-ROM (❶), and then the other twelve screws locking the base unit frame. (figure 2-11) Now you can lift the base unit frame up.

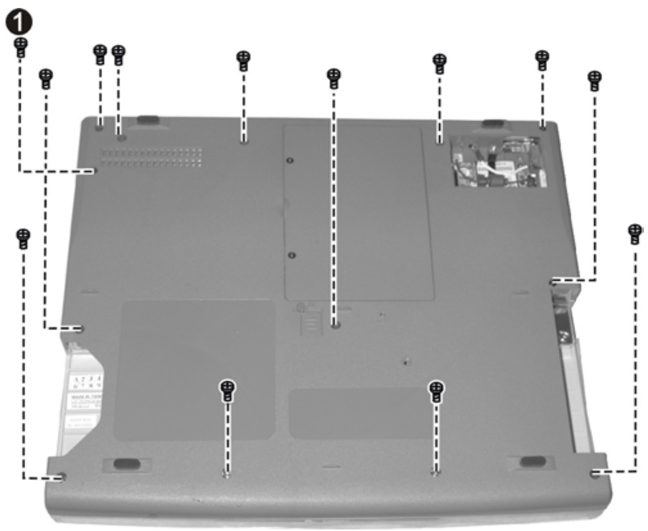


Figure 2-11

6. Hold the CD-ROM drive and slide it outward carefully. (figure 2-12).

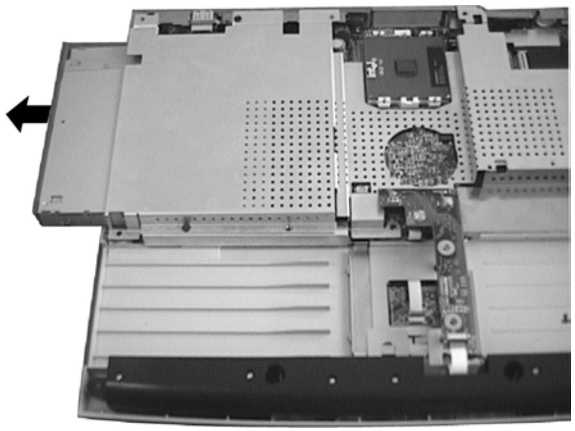


Figure 2-12

Reassembly

1. Push the CD-ROM drive into the compartment.
2. Replace the base unit frame and secure with thirteen screws (includes one locking the CD-ROM drive).
3. Replace the FDD/HDD module. (See section 2.2.4 Reassembly.)
4. Replace the modem card. (See section 2.2.3 Reassembly.)
5. Replace the modem card. (See section 2.2.3 Reassembly.)
6. Replace the battery pack. (See section 2.2.1 Reassembly.)

2.2.6 Keyboard

Disassembly

1. Open the top cover.
2. Press the locking latch downward to unlatch the Easy Start panel (❶) , push it leftward and lift it up from the left side (❷). (figure 2-13)



Figure 2-13

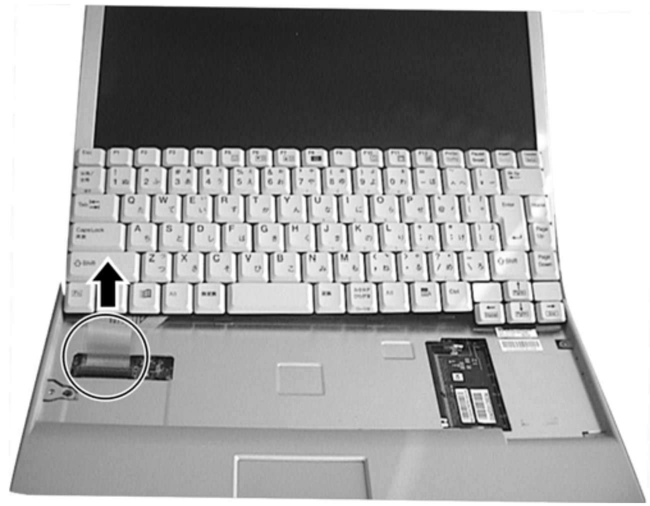


Figure 2-14

3. Slightly lift up the keyboard and disconnect the cable from the system board to detach the keyboard.

Reassembly

1. Reconnect the keyboard cable and fit the keyboard back into place.
2. Replace the Easy Start panel.

2.2.7 SO-DIMM

Disassembly

1. Remove the keyboard to access the SO-DIMM sockets. (See section 2.2.6 Disassembly.)
2. Pull the retaining clips outwards (❶) and remove the SO-DIMM (❷). (figure 2-15)

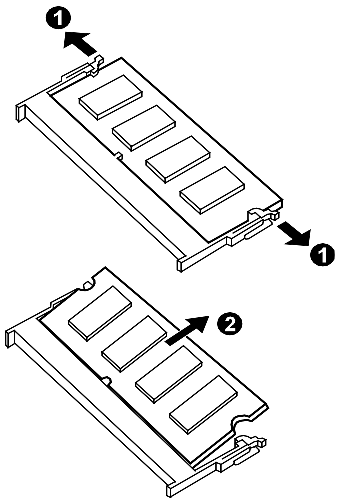


Figure 2-15

Reassembly

1. To install the SO-DIMM, match the SO-DIMM's notched part with the socket's projected part and firmly insert the SO-DIMM into the socket at 20-degree angle. Then push down until the retaining clips lock the SO-DIMM into position.
2. Replace the keyboard and the Easy Start panel. (See section 2.2.6 Reassembly.)

2.2.8 LCD Assembly

Disassembly

1. Open the top cover and remove the Easy Start panel. (See steps 1 to 2 in section 2.2.6 Disassembly.)
2. Remove the two hinge covers by inserting a flat screwdriver to the rear of the cover and pry the cover out. (figure 2-16)



Figure 2-16



Figure 2-17

3. Open the top cover. Unplug the three cable connectors coming from the LCD assembly, and remove four screws of the hinges. Now you can separate the LCD assembly from the base unit. (figure 2-17)

Reassembly

1. Attach the LCD assembly to the base unit and secure with four screws on the hinges.
2. Reconnect the LCD cable connectors to the system board.
3. Replace the two hinge covers.
4. Replace the Easy Start panel.

2.2.9 LCD Panel

Disassembly

1. Remove the LCD assembly. (See section 2.2.8 Disassembly.)
2. Remove the two rubber pads and two screws on the lower part of the panel. (figure 2-18)



Figure 2-18



Figure 2-19

3. Insert a flat screwdriver to the lower part of the frame and gently pry the frame out.
   Repeat the process until the frame is completely separated from the housing.
4. Remove the four screws on the two sides of the LCD panel, and unplug the cable from
   the inverter board. (figure 2-19)

Reassembly

1. Fit the LCD panel back into place and secure with four screws, and reconnect the cable to the inverter board.
2. Fit the LCD frame back into the housing and replace the two screws and two rubber pads.
3. Replace the LCD assembly. (See section 2.2.8 Reassembly.)

2.2.10 Inverter Board

Disassembly

1. Remove the LCD assembly and detach the LCD frame (see instructions in previous two sections).
2. To remove the inverter board at the bottom side of the LCD assembly, unplug the cable and remove the two screws. (figure 2-20)

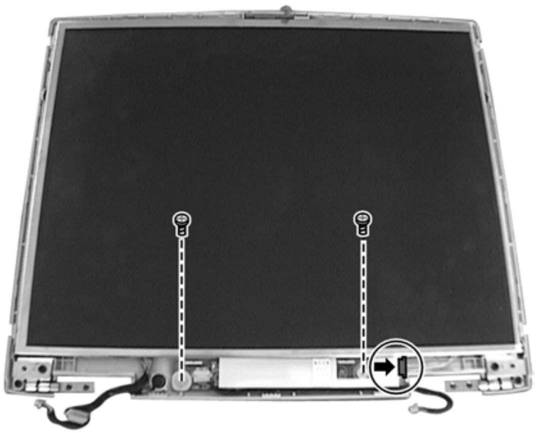


Figure 2-20

Reassembly

1. Fit the inverter board back into place and secure with two screws.
2. Reconnect the cables.
3. Replace the LCD frame. (See section 2.2.9 Reassembly.)
4. Replace the LCD assembly. (See section 2.2.8 Reassembly.)

2.2.11 System Board

Disassembly

1. Remove the Keyboard. (See section 2.2.6 Disassembly.)
2. Remove the LCD assembly. (See section 2.2.8 Disassembly.)
3. Remove seven screws, and then take out the Easy Start board. (figure 2-21)

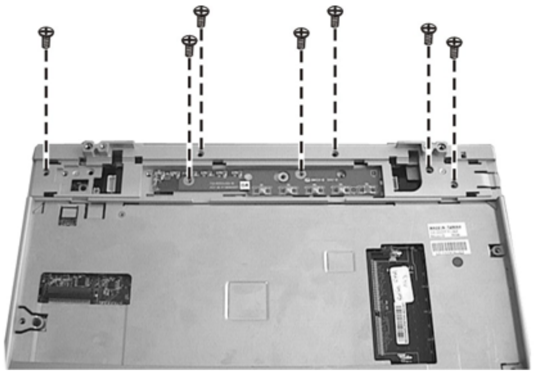


Figure 2-21



Figure 2-22

4. Remove four screws on the rear side of the notebook. (figure 2-22)
5. Remove the battery pack, heatsink, modem card, FDD/HDD module, and CD-ROM drive.
   (See section 2.2.1 to 2.2.5 Disassembly.)

6. Remove six screws and two hexnut screws fastening the metal shield, and then lift the shield up from the system board carefully. (figure 2-23)

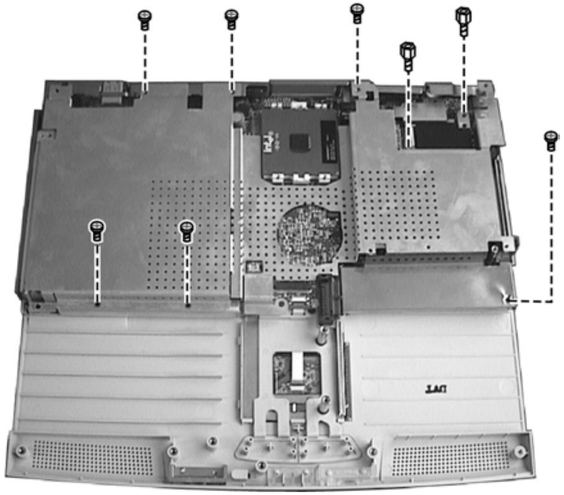


Figure 2-23

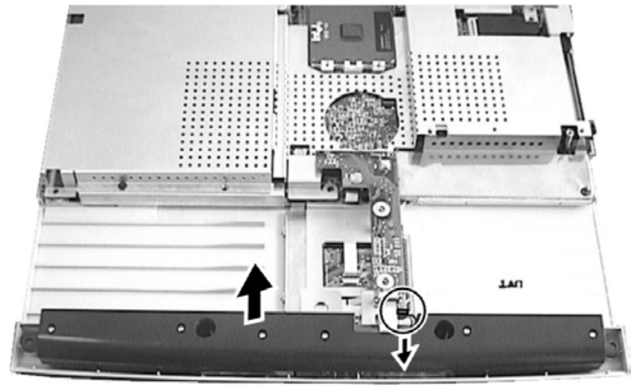


Figure 2-24

7. Lift up the speaker assembly and disconnect the cable. (figure 2-24)

8. Remove four screws to take the recharge board apart. (figure 2-25)

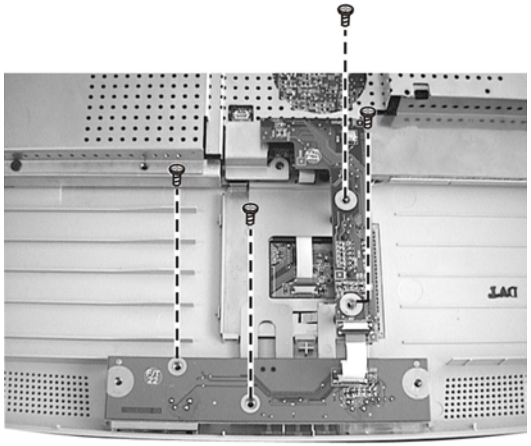


Figure 2-25

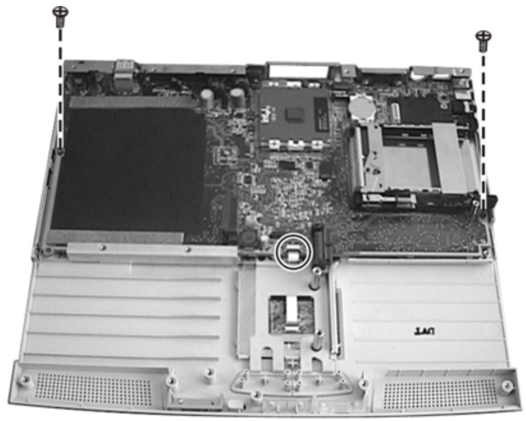


Figure 2-26

9. Remove two screws fastening the system board and disconnect the cable of the touchpad. Now you can lift the system board up from the base unit. (figure 2-26)

Reassembly

1. Fit the system board into place and secure with two screws.
2. Reconnect the touchpad's cable.
3. Replace the metal shield and secure with six screws and two hexnut screws.
4. Replace the recharge board and secure with four screws.
5. Replace the speaker assembly and reconnect the cable.

6. Replace the base unit frame and secure with twelve screws.
7. Replace the battery pack, heatsink, modem card, FDD/HDD module, and CD-ROM drive.
8. Secure the four screws on the rear side of the notebook.
9. Put the notebook back to the upright position. Replace the Easy Start board into the housing, then secure with seven screws.
10. Replace the LCD assembly.
11. Replace the keyboard and Easy Start panel.

2.2.12 Touchpad

Disassembly

1. Remove the system board. (See section 2.2.11 Disassembly.)
2. Remove the four screws to lift up the touchpad holder and touchpad panel. (figure 2-27)

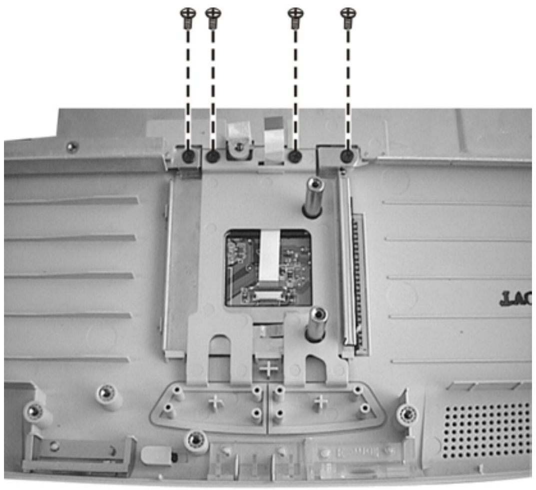


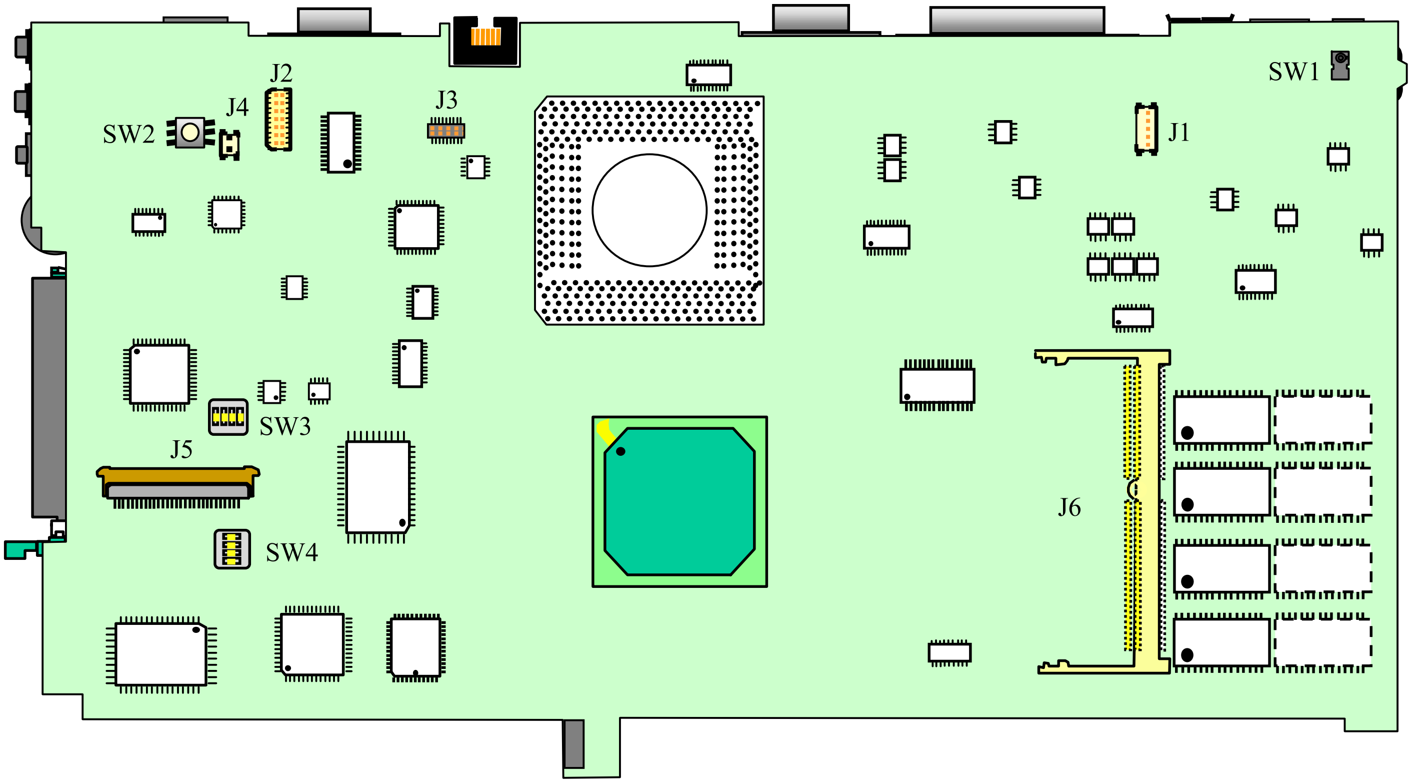
Figure 2-27

Reassembly

1. Replace the touchpad holder and touchpad panel, and secure with four screws.
2. Replace the system board and assemble the notebook. (See section 2.2.11 Reassembly.)

3. Definition & Location Of Connectors / Switches

3.1 Mother Board-A



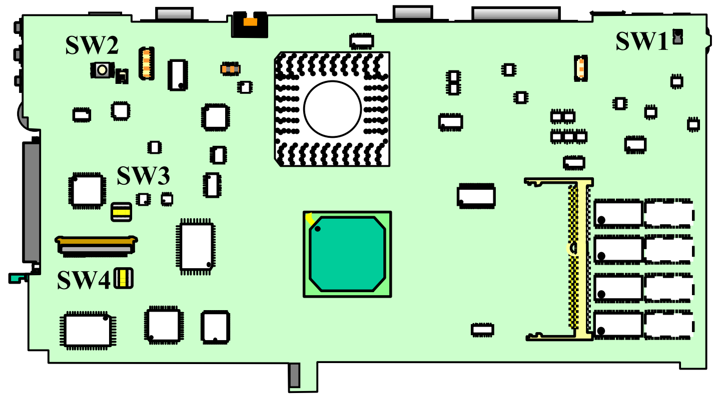
- J1: Inverter BD CONN.
- J2: LCD panel LVDS connector.
- J3: ESB Board connector.
- J4: External MIC-in connector.
- J5: Internal keyboard connector.
- J6: 144 pins expansion SDRAM SO-DIMM socket.
- SW1: Cover Suspend Switch.
- SW2: Power button.
- SW3 : CPU FSB Select.
- SW4 : LCD Panel ID Select.

3. Definition & Location Of Connectors / Switches

3.2 Mother Board Switch Table

SW3. CPU & SDRAM Frequency setting table:

SW_FS3	SW_FS2	SW_FS1	SW_FS0	CPU	SDRAM
0	0	0	0	66	100
0	0	0	1	100	100
0	0	1	1	133	100
0	1	0	0	66	133
0	1	0	1	100	133
0	1	1	1	133	133
1	0	0	0	66	66



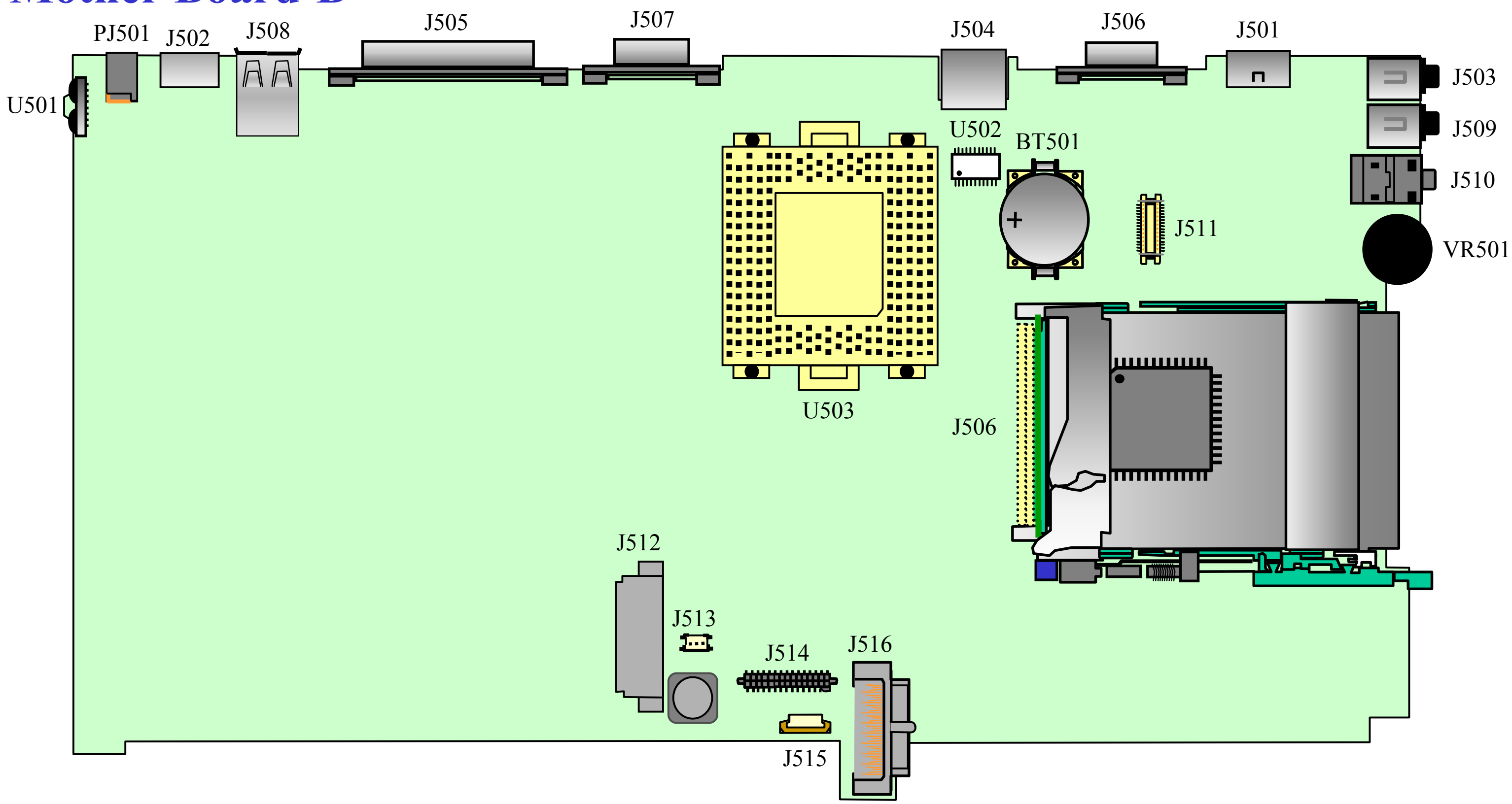
SW4. LCD Panel ID Select

LCD_SW4	LCD_SW3	LCD_SW2	LCD_SW1	Vendor	PANEL	Description
0	0	0	0	HannStar	HSD141PX11	14.1”
0	0	0	1	Unipac	UP141X01-2	14.1”
0	0	1	0	Hyundai	14X13-101	14.1”
1	0	0	0	Hyundai	HT15X31	15”
1	0	0	1	Hitachi	TX38D85VC1CAA	15”

7521Plus / N N/B MAINTENANCE

3. Definition & Location Of Connectors / Switches

3.3 Mother Board-B

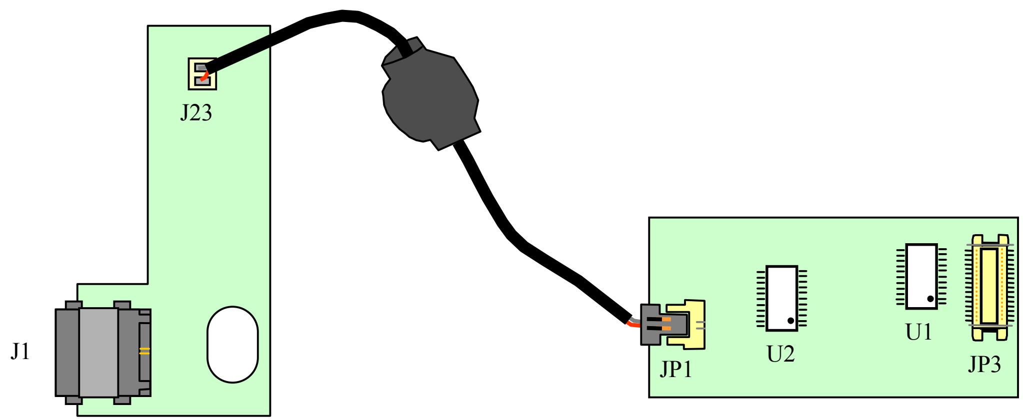


- PJ501: Power jack (AC adapter).
- J502 : PS2 Mouse/keyboard.
- J503: Line in Jack.
- J504: RJ45 LAN connect.
- J505: Parallel Port.
- J506: PCMCIA card socket.
- J507: VGA Connector.
- J508: USB connector.
- J509: Phone Jack Connector.
- J510: Line Out with APDIF.
- J511: MDC MODEM transfer BD connector.
- J513: CPU FAN Connector.
- J516 :HDD/FDD Connector.
- J512: CD-ROM drive connector.
- J514: Charger & Touch-Pad connector.
- J515: Touch-Pad button connector.
- BT501: CMOS Battery connector.
- VR501: Volume control VR.
- U503: FC-PGA Socket 370 CPU Slot.

3. Definition & Location Of Connectors / Switches

3.4 Daughter Board

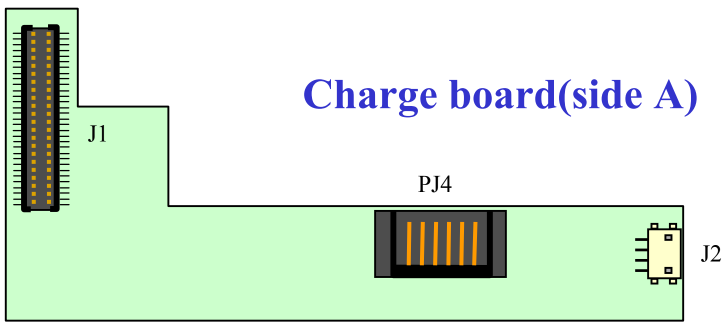
MDC/LAN transfer board

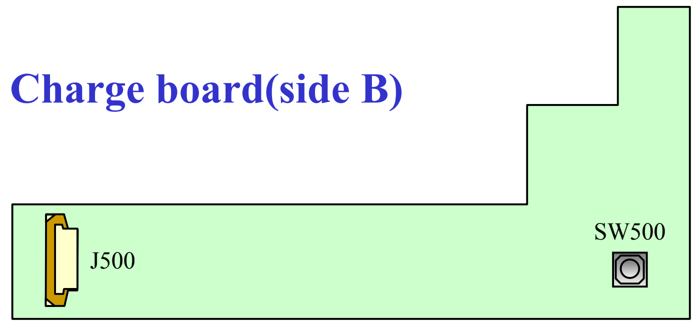


- J1: RJ-11 phone jack for internal modem.
- J23: MDC jump wire connector.
- JP1: MDC jump wire connector.
- JP3: Connector 2 for connected MDC/LAN transfer board to M/B.

3. Definition & Location Of Connectors / Switches

3.5 Charger Board



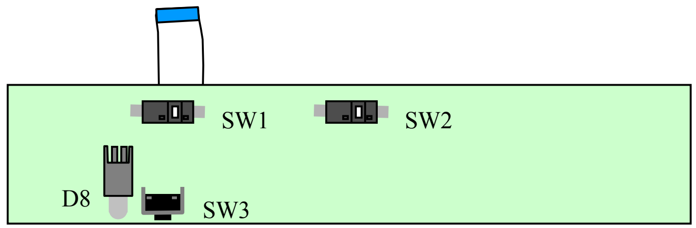


- J1:Charger & Touch-Pad connector to M/B.
- PJ4:Battery pack connector.
- J2: Internal speaker connector.
- J500: Touch-Pad button connector.
- SW500: CMOS Reset

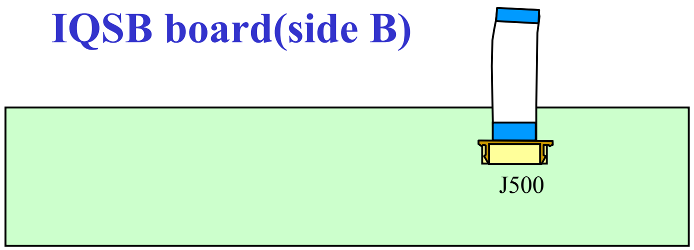
3. Definition & Location Of Connectors / Switches

3.6 IQSB Board

IQSB board(side A)



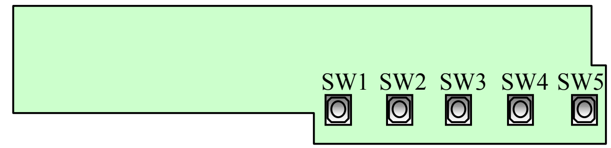
IQSB board(side B)



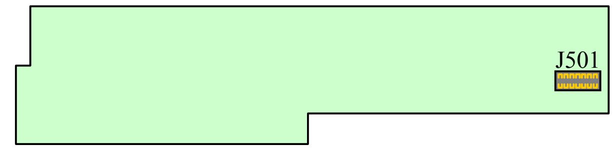
- SW1: Touch Pad Left Key.
- SW2: Touch Pad Left Key.
- SW3: E-Mail Function key.
- D8: E-Mail Indicator LED.
- J500: IQSB Board to MB J515 Touch-Pad Button Connector.

3.7 Easy Start Button Board

Easy Start Button Board(side A)



Easy Start Button Board(side B)

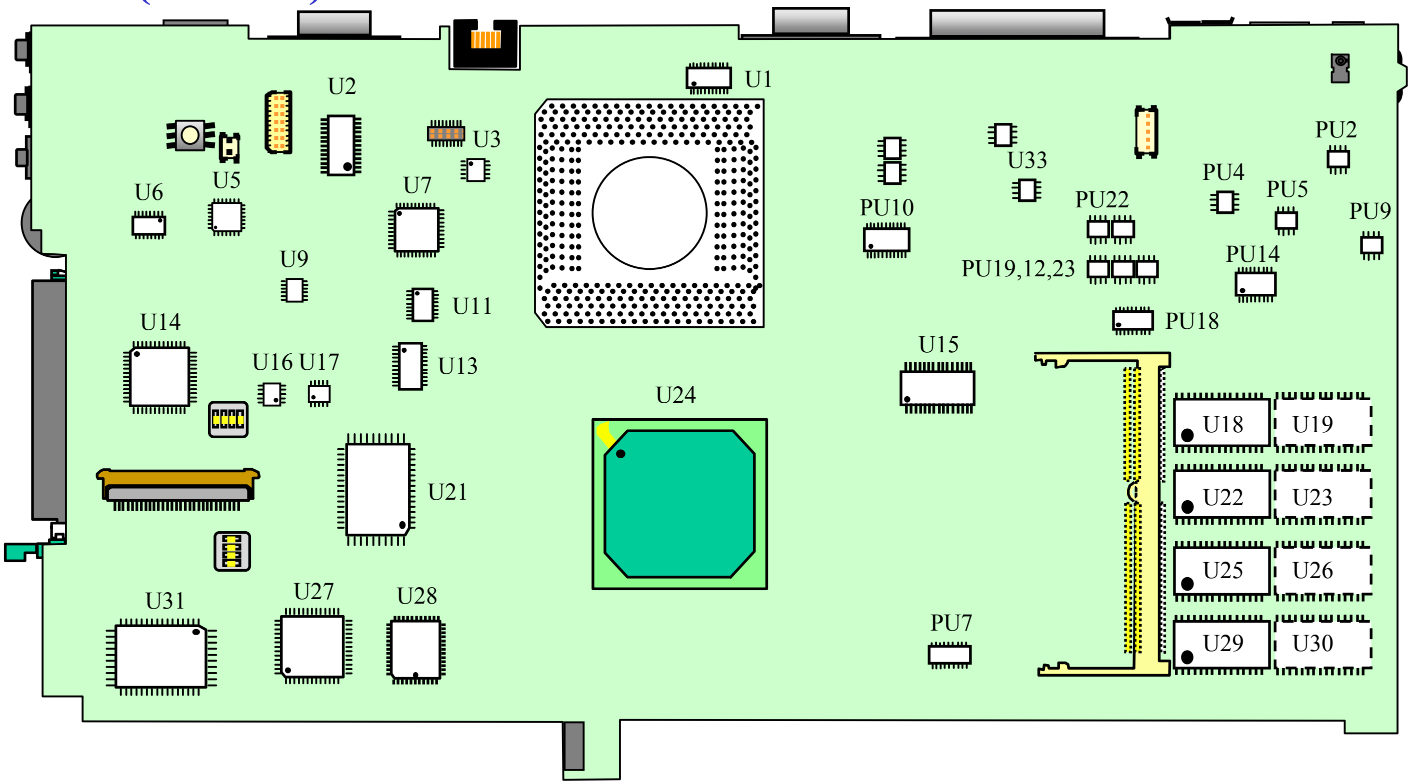


- J501: Easy Start Button Board to MB Connector .
- SW1,SW2,SW3,SW4,SW5,SW6:

  Programmable Easy Start Button function key.

4. Definition & Location Of Major Components

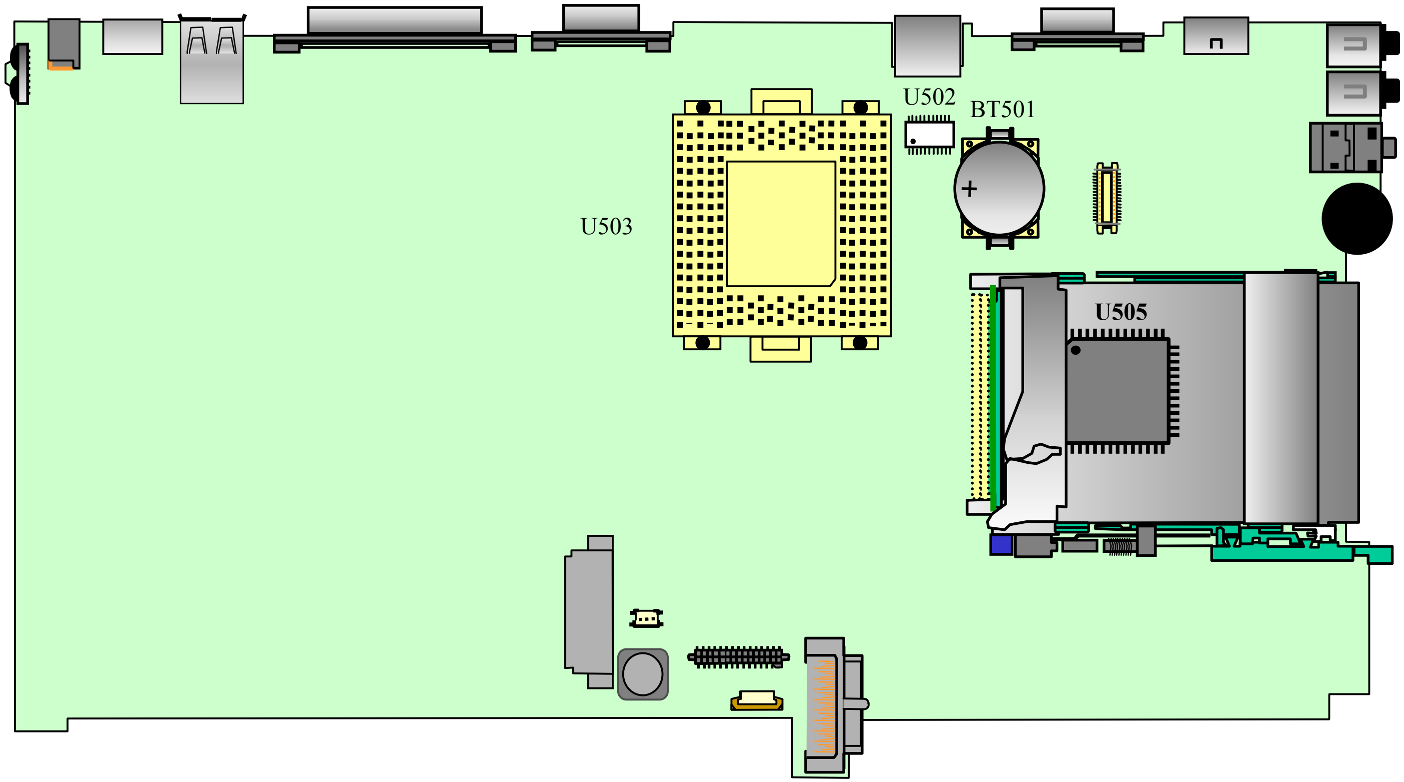
4.1 Main Board (Side A)



- U1: ADM3311ARU RS232/SIO.
- U2: DS90C363MTD VGA LVD controller.
- U5: CS4299 AC'97 CODE.
- U6: TPA0202 AUDIO AMP.
- U7: CH7005C TV-Encoder.
- U14: H8(3434F) universal.
- U13: TPS2206 PCcard Power switch matrix.
- U15: ICS9248-102 Frequency Synthesizer.
- U24: SiS630S single chipset.
- U27: Super IO PC97338VJG.
- U28: System BIOS.
- U31:W83626F LPC to ISA.
- U18,U22,U25,U29 : On board SDAM.

4. Definition & Location Of Major Components

4.2 Main Board (SIDE B)



- U502: PH163112 LAN Controller.
- U503: Socket 370 CPU.
- U505: PCI1225PDV PC CARD interface controller.

5. Pin Descriptions Of Major Components

5.1 Pentium III/Celeron FC-PGA2 CPU

Alphabetical Signal Reference

Signal Name	I/O	Signal Description
A[35:3]#	I/O GTL+	The A[35:3]# (Address) signals define a 2^{36}-byte physical memory address space. When ADS# is active, these signals transmit the address of a transaction; when ADS# is inactive, these signals transmit transaction information. These signals must be connected to the appropriate pins/balls of both agents on the system bus. The A[35:24]# signals are protected with the AP1# parity signal, and the A[23:3]# signals are protected with the AP0# parity signal. On the active-to-inactive transition of RESET#, each processor bus agent samples A[35:3]# signals to determine its power-on configuration. See Section 4 of this document and the *PentiumII Processor Developer's Manual* for details.
A20M#	I 1.5V Tolerant	If the A20M# (Address-20 Mask) input signal is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in Real mode.
ADS#	I/O GTL+	The ADS# (Address Strobe) signal is asserted to indicate the validity of a transaction address on the A[35:3]# signals. Both bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop or deferred reply ID match operations associated with the new transaction. This signal must be connected to the appropriate pins/balls on both agents on the system bus.
AERR#	I/O GTL+	The AERR# (Address Parity Error) signal is observed and driven by both system bus agents, and if used, must be connected to the appropriate pins/balls of both agents on the system bus. AERR# observation is optionally enabled during power-on configuration; if enabled, a valid assertion of AERR# aborts the current transaction. If AERR# observation is disabled during power-on configuration, a central agent may handle an assertion of AERR# as appropriate to the error handling architecture of the system.
AP[1:0]#	I/O GTL+	The AP[1:0]# (Address Parity) signals are driven by the request initiator along with ADS#, A[35:3]#, REQ[4:0]# and RP#. AP1# covers A[35:24]#. AP0# covers A[23:3]#. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This allows parity to be high when all the covered signals are high. AP[1:0]# should be connected to the appropriate pins/balls on both agents on the system bus.
BCLK	I 2.5V Tolerant	The BCLK (Bus Clock) signal determines the system bus frequency. Both system bus agents must receive this signal to drive their outputs and latch their inputs on the BCLK rising edge. All external timing parameters are specified with respect to the BCLK signal.

Signal Name	I/O	Signal Description
BERR#	I/O GTL+	The BERR# (Bus Error) signal is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by either system bus agent and must be connected to the appropriate pins/balls of both agents, if used. However, the mobile Pentium III processors do not observe assertions of the BERR# signal. BERR# assertion conditions are defined by the system configuration. Configuration options enable the BERR# driver as follows: • Enabled or disabled • Asserted optionally for internal errors along with IERR# • Asserted optionally by the request initiator of a bus transaction after it observes an error • Asserted by any bus agent when it observes an error in a bus transaction
BINIT#	I/O- GTL+	The BINIT# (Bus Initialization) signal may be observed and driven by both system bus agents and must be connected to the appropriate pins/balls of both agents, if used. If the BINIT# driver is enabled during the power-on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future information. If BINIT# is enabled during power-on configuration, and BINIT# is sampled asserted, all bus state machines are reset and any data which was in transit is lost. All agents reset their rotating ID for bus arbitration to the state after reset, and internal count information is lost. The L1 and L2 caches are not affected. If BINIT# is disabled during power-on configuration, a central agent may handle an assertion of BINIT# as appropriate to the Machine Check Architecture (MCA) of the system.
BNR#	I/O- GTL+	The BNR# (Block Next Request) signal is used to assert a bus stall by any bus agent that is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions. Since multiple agents may need to request a bus stall simultaneously, BNR# is a wired-OR signal that must be connected to the appropriate pins/balls of both agents on the system bus. In order to avoid wire-OR glitches associated with simultaneous edge transitions driven by multiple drivers, BNR# is activated on specific clock edges and sampled on specific clock edges.
BP[3:2]#	I/O GTL+	The BP[3:2]# (Breakpoint) signals are the System Support group Breakpoint signals. They are outputs from the processor that indicate the status of breakpoints.
BPM[1:0]#	I/O GTL+	The BPM[1:0]# (Breakpoint Monitor) signals are breakpoint and performance monitor signals. They are outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance.

5. Pin Descriptions Of Major Components

5.1 Pentium III/Celeron FC-PGA2 CPU

Alphabetical Signal Reference

Signal Name	I/O	Signal Description
BPRI#	I GTL+	The BPRI# (Bus Priority Request) signal is used to arbitrate for ownership of the system bus. It must be connected to the appropriate pins/balls on both agents on the system bus. Observing BPRI# active (as asserted by the priority agent) causes the processor to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed and then releases the bus by deasserting BPRI#.
BREQ0#	I/O GTL+	The BREQ0# (Bus Request) signal is a processor Arbitration Bus signal. The processor indicates that it wants ownership of the system bus by asserting the BREQ0# signal. During power-up configuration, the central agent must assert the BREQ0# bus signal. The processor samples BREQ0# on the active-to-inactive transition of RESET#.
BSEL[1:0]	I 1.5V Tolerant	The BSEL[1:0] (Select Processor System Bus Speed) signal is used to configure the processor for the system bus frequency. Table 38 shows the encoding scheme for BSEL[1:0]. The only supported system bus frequency for the mobile Pentium III processor is 100 MHz. If another frequency is used or if the BSEL[1:0] signals are not driven with "1" then the processor is not guaranteed to function properly. **BSEL[1:0] Encoding** **BSEL[1:0]** — **System Bus Frequency** 00 — 66 MHz 01 — 100 MHz 10 — Reserved 11 — 133 MHz
CLKREF	Analog	The CLKREF (System Bus Clock Reference) signal provides a reference voltage to define the trip point for the BCLK signal. This signal should be connected to a resistor divider to generate 1.25V from the 2.5-V supply.
CMOSREF	Analog	The CMOSREF (CMOS Reference Voltage) signal provides a DC level reference voltage for the CMOS input buffers. A voltage divider should be used to divide a stable voltage plane (e.g., 2.5V or 3.3V). This signal must be provided with a DC voltage that meets the VCMOSREF specification from Table 13.
D[63:0]#	I/O GTL+	The D[63:0]# (Data) signals are the data signals. These signals provide a 64-bit data path between both system bus agents, and must be connected to the appropriate pins/balls on both agents. The data driver asserts DRDY# to indicate a valid data transfer.

Signal Name	I/O	Signal Description
DBSY#	I/O- GTL+	The DBSY# (Data Bus Busy) signal is asserted by the agent responsible for driving data on the system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must be connected to the appropriate pins/balls on both agents on the system bus.
DEFER#	I GTL+	The DEFER# (Defer) signal is asserted by an agent to indicate that the transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory agent or I/O agent. This signal must be connected to the appropriate pins/balls on both agents on the system bus.
DEP[7:0]#	I/O GTL+	The DEP[7:0]# (Data Bus ECC Protection) signals provide optional ECC protection for the data bus. They are driven by the agent responsible for driving D[63:0]#, and must be connected to the appropriate pins/balls on both agents on the system bus if they are used. During power-on configuration, DEP[7:0]# signals can be enabled for ECC checking or disabled for no checking.
DRDY#	I/O GTL+	The DRDY# (Data Ready) signal is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-cycle data transfer, DRDY# can be deasserted to insert idle clocks. This signal must be connected to the appropriate pins/balls on both agents on the system bus.
EDGCTRLP	Analog	The EDGCTRLP (Edge Rate Control) signal is used to configure the edge rate of the GTL+ output buffers. Connect the signal to VSS with a 110-Ω, 1% resistor.
FERR#	O 1.5V Tolerant Open- drain)	The FERR# (Floating-point Error) signal is asserted when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and it is included for compatibility with systems using DOS-type floating-point error reporting.
FLUSH#	I 1.5V Tolerant	When the FLUSH# (Flush) input signal is asserted, the processor writes back all internal cache lines in the Modified state and invalidates all internal cache lines. At the completion of a flush operation, the processor issues a Flush Acknowledge transaction. The processor stops caching any new data while the FLUSH# signal remains asserted. On the active-to-inactive transition of RESET#, each processor bus agent samples FLUSH# to determine its power-on configuration.

5. Pin Descriptions Of Major Components

5.1 Pentium III/Celeron FC-PGA2 CPU

Alphabetical Signal Reference

Signal Name	I/O	Signal Description
GHI#	I 1.5V Tolerant	The GHI# signal controls which operating mode bus ratio is selected in a mobile Pentium III processor featuring Intel SpeedStep technology. On the processor featuring Intel SpeedStep technology, this signal is latched when BCLK restarts in Deep Sleep state and determines which of two bus ratios is selected for operation. This signal is ignored when the processor is not in the Deep Sleep state. This signal is a "Don't Care" on processors that do not feature Intel SpeedStep technology. This signal has an on-die pull-up to VccT and should be driven with an Open-drain driver with no external pull-up.
HIT#, HITM#	I/O GTL+	The HIT# (Snoop Hit) and HITM# (Hit Modified) signals convey transaction snoop operation results, and must be connected to the appropriate pins/balls on both agents on the system bus. Either bus agent can assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	O 1.5V Tolerant Open-drain	The IERR# (Internal Error) signal is asserted by the processor as the result of an internal error.Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system logic. The processor will keep IERR# asserted until it is handled in software or with the assertion of RESET#, BINIT, or INIT#.
IGNNE#	I 1.5V Tolerant	The IGNNE# (Ignore Numeric Error) signal is asserted to force the processor to ignore a numeric error and continue to execute non-control floating-point instructions. If IGNNE# is deasserted, the processor freezes on a non-control floating-point instruction if a previous instruction caused an error. IGNNE# has no affect when the NE bit in control register 0 (CR0) is set.
INIT#	I 1.5V Tolerant	The INIT# (Initialization) signal is asserted to reset integer registers inside the processor without affecting the internal (L1 or L2) caches or the floating-point registers. The processor begins execution at the power-on reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous input. If INIT# is sampled active on RESET#'s active-to-inactive transition, then the processor executes its built-in self test (BIST).

Signal Name	I/O	Signal Description
INTR	I 1.5V Tolerant	The INTR (Interrupt) signal indicates that an external interrupt has been generated. INTR becomes the LINT0 signal when the APIC is enabled. The interrupt is maskable using the IF bit in the EFLAGS register. If the IF bit is set, the processor vectors to the interrupt handler after completing the current instruction execution. Upon recognizing the interrupt request, the processor issues a single Interrupt Acknowledge (INTA) bus transaction. INTR must remain active until the INTA bus transaction to guarantee its recognition.
LINT[1:0]	I 1.5V Tolerant	The LINT[1:0] (Local APIC Interrupt) signals must be connected to the appropriate pins/balls of all APIC bus agents, including the processor and the system logic or I/O APIC component. When APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a non-maskable interrupt. INTR and NMI are backward compatible with the same signals for the Pentium processor. Both signals are asynchronous inputs. Both of these signals must be software configured by programming the APIC register space to be used either as NMI/INTR or LINT[1:0] in the BIOS. If the APIC is enabled at reset, then LINT[1:0] is the default configuration.
LOCK#	I/O GTL+	The LOCK# (Lock) signal indicates to the system that a sequence of transactions must occur atomically. This signal must be connected to the appropriate pins/balls on both agents on the system bus. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction through the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for bus ownership, it waits until it observes LOCK# deasserted. This enables the processor to retain bus ownership throughout the bus locked operation and guarantee the atomicity of lock.
NMI	I 1.5V Tolerant	The NMI (Non-Maskable Interrupt) indicates that an external interrupt has been generated. NMI becomes the LINT1 signal when the APIC is disabled. Asserting NMI causes an interrupt with an internally supplied vector value of 2. An external interrupt-acknowledge transaction is not generated. If NMI is asserted during the execution of an NMI service routine, it remains pending and is recognized after the IRET is executed by the NMI service routine. At most, one assertion of NMI is held pending. NMI is rising edge sensitive.

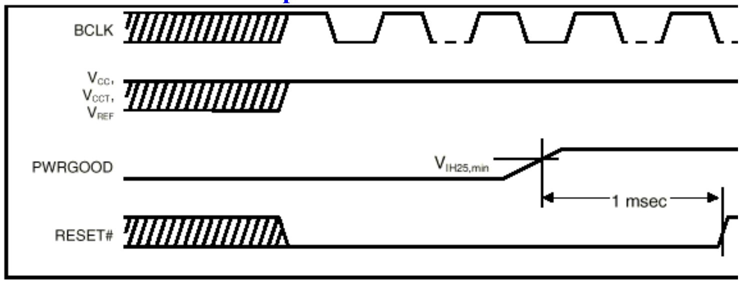
5. Pin Descriptions Of Major Components

5.1 Pentium III/Celeron FC-PGA2 CPU

Alphabetical Signal Reference

Signal Name	I/O	Signal Description
PICCLK	I 2.5V Tolerant	The PICCLK (APIC Clock) signal is an input clock to the processor and system logic or I/O APIC that is required for operation of the processor, system logic, and I/O APIC components on the APIC bus.
PICD[1:0]	I/O 1.5V Tolerant Open-drain	The PICD[1:0] (APIC Data) signals are used for bi-directional serial message passing on the APIC bus. They must be connected to the appropriate pins/balls of all APIC bus agents, including the processor and the system logic or I/O APIC components. If the PICD0 signal is sampled low on the active-to-inactive transition of the RESET# signal, then the APIC is hardware disabled.
PLL1, PLL2	Analog	The PLL1 and PLL2 signals provide isolated analog decoupling is required for the internal PLL. See Section 3.2.2 for a description of the analog decoupling circuit.
PRDY#	O GTL+	The PRDY# (Probe Ready) signal is a processor output used by debug tools to determine processor debug readiness.
PREQ#	I 1.5V Tolerant	The PREQ# (Probe Request) signal is used by debug tools to request debug operation of the processor.
PWRGOOD	I 2.5V Tolerant	PWRGOOD (Power Good) is a 2.5-V tolerant input. The processor requires this signal to be a clean indication that clocks and the power supplies (Vcc, VccT, etc.) are stable and within their specifications. Clean implies that the signal will remain low, (capable of sinking leakage current) and without glitches, from the time that the power supplies are turned on, until they come within specification. The signal will then transition monotonically to a high (2.5V) state. Figure 26 illustrates the relationship of PWRGOOD to other system signals. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before the rising edge of PWRGOOD. It must also meet the minimum pulse width specified in Table 17 (Section 3.7) and be followed by a 1 ms RESET# pulse.

PWRGOOD Relationship at Power On



PWRGOOD Relationship at Power On

The PWRGOOD signal, which must be supplied to the processor, is used to protect internal circuits against voltage sequencing issues. The PWRGOOD signal should be driven high throughout boundary scan operation.

Signal Name	I/O	Signal Description
REQ[4:0]#	I/O GTL+	The REQ[4:0]# (Request Command) signals must be connected to the appropriate pins/balls on both agents on the system bus. They are asserted by the current bus owner when it drives A[35:3]# to define the currently active transaction type.
RESET#	I GTL+	Asserting the RESET# signal resets the processor to a known state and invalidates the L1 and L2 caches without writing back Modified (M state) lines. For a power-on type reset, RESET# must stay active for at least 1 msec after Vcc and BCLK have reached their proper DC and AC specifications and after PWRGOOD has been asserted. When observing active RESET#, all bus agents will deassert their outputs within two clocks. RESET# is the only GTL+ signal that does not have on-die GTL+ termination. A 56.2Ω1% terminating resistor connected to VccT is required. A number of bus signals are sampled at the active-to-inactive transition of RESET# for the power-on configuration. The configuration options are described in Section 4 and in the *Pentium II Processor Developer's Manual*. Unless its outputs are tri-stated during power-on configuration, after an active-to-inactive transition of RESET#, the processor optionally executes its built-in self-test (BIST) and begins program execution at reset-vector 000FFFF0H or FFFFFFF0H. RESET# must be connected to the appropriate pins/balls on both agents on the system bus.
RP#	I/O GTL+	The RP# (Request Parity) signal is driven by the request initiator and provides parity protection on ADS# and REQ[4:0]#. RP# should be connected to the appropriate pins/balls on both agents on the system bus. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This definition allows parity to be high when all covered signals are high.
RS[2:0]#	I GTL+	The RS[2:0]# (Response Status) signals are driven by the response agent (the agent responsible for completion of the current transaction) and must be connected to the appropriate pins/balls on both agents on the system bus.

5. Pin Descriptions Of Major Components

5.1 Pentium III/Celeron FC-PGA2 CPU

PWRGOOD Relationship at Power On

Signal Name	I/O	Signal Description
RSP#	I GTL+	The RSP# (Response Parity) signal is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#. RSP# provides parity protection for RS[2:0]#. RSP# should be connected to the appropriate pins/balls on both agents on the system bus. A correct parity signal is high if an even number of covered signals are low, and it is low if an odd number of covered signals are low. During Idle state of RS[2:0]# (RS[2:0]#=000), RSP# is also high since it is not driven by any agent guaranteeing correct parity.
RSVD	TBD	The RSVD (Reserved) signal is currently unimplemented but is reserved for future use. Leave this signal unconnected. Intel recommends that a routing channel for this signal be allocated.
RTTIMPEDP	Analog	The RTTIMPEDP (RTT Impedance/PMOS) signal is used to configure the on-die GTL+ termination. Connect the RTTIMPEDP signal to VSS with a 56.2-Ω, 1% resistor.
SLP#	I 1.5V Tolerant	The SLP# (Sleep) signal, when asserted in the Stop Grant state, causes the processor to enter the Sleep state. During the Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still running. The processor will not recognize snoop and interrupts in the Sleep state. The processor will only recognize changes in the SLP#, STPCLK# and RESET# signals while in the Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to the Stop Grant state in which it restarts its internal clock to the bus and APIC processor units.
SMI#	I 1.5V Tolerant	The SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enters System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler.
STPCLK#	I 1.5V Tolerant	The STPCLK# (Stop Clock) signal, when asserted, causes the processor to enter a low-power Stop Grant state. The processor issues a Stop Grant Acknowledge special transaction and stops providing internal clock signals to all units except the bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in the Stop Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no affect on the bus clock.
TCK	I 1.5V Tolerant	The TCK (Test Clock) signal provides the clock input for the test bus (also known as the test access port).

Signal Name	I/O	Signal Description
TDI	I 1.5V Tolerant	The TDI (Test Data In) signal transfers serial test data to the processor. TDI provides the serial input needed for JTAG support.
TDO	O 1.5V Tolerant Open-drain	The TDO (Test Data Out) signal transfers serial test data from the processor. TDO provides the serial output needed for JTAG support.
TESTHI	I 1.5V Tolerant	The TESTHI (Test input High) is used during processor test and needs to be pulled high during normal operation.
TESTLO[2:1]	I 1.5V Tolerant	The TESTLO[2:1] (Test input Low) signals are used during processor test and needs to be pulled to ground during normal operation.
TESTP	Analog	The TESTP (Test Point) signals are connected to Vcc and Vss at opposite ends of the die. These signals can be used to monitor the Vcc level on the die. Route the TESTP signals to test points or leave them unconnected. Do not short the TESTP signals together.
THERMDA, THERMDC	Analog	The THERMDA (Thermal Diode Anode) and THERMDC (Thermal Diode Cathode) signals connect to the anode and cathode of the on-die thermal diode.
TMS	I 1.5V Tolerant	The TMS (Test Mode Select) signal is a JTAG support signal used by debug tools.
TRDY#	I GTL+	The TRDY# (Target Ready) signal is asserted by the target to indicate that the target is ready to receive write or implicit write-back data transfer. TRDY# must be connected to the appropriate pins/balls on both agents on the system bus.
TRST#	I 1.5V Tolerant	The TRST# (Test Reset) signal resets the Test Access Port (TAP) logic. The mobile Pentium III processors do not self-reset during power on; therefore, it is necessary to drive this signal low during power-on reset.

5. Pin Descriptions Of Major Components

5.1 Pentium III/Celeron FC-PGA2 CPU

PWRGOOD Relationship at Power On

Signal Name	I/O	Signal Description
VID[4:0]	O - Open-drain	The VID[4:0] (Voltage ID) pins/balls can be used to support automatic selection of power supply voltages. These pins/balls are not signals, they are either an open circuit or a short to VSS on the processor substrate. The combination of opens and shorts encodes the voltage required by the processor. External to pull-ups are required to sense the encoded VID. For processors that have Intel SpeedStep technology enabled, VID[4:0] encode the voltage required in the battery-optimized mode. VID[4:0] are needed to cleanly support voltage specification changes on mobile Pentium III processors. The voltage encoded by VID[4:0] is defined in Table 39. A "1" in this table refers to an open pin/ball and a "0" refers to a short to VSS. The power supply must provide the requested voltage or disable itself. Please note that in order to implement VID on the BGA2 package, some VID[4:0] balls may be depopulated. For the BGA2 package, a "1" in Table 39 implies that the corresponding VID ball is depopulated, while a "0" implies that the corresponding VID ball is not depopulated. But on the Micro-PGA2 package, VID[4:0] pins are not depopulated.

5. Pin Descriptions Of Major Components

5.2 SiS630S Slot 1/Socket 370 2D/3D Ultra-AGP™ Single Chipset

Host Bus Interface

Name	Tolerance	Power Plane	Type Attr	Description
CPUCLK	3.3V/5V	MAIN	I	**Host Clock :**
ADS#	1.5V	MAIN	I/O GTL+	**Address Strobe :** Address Strobe is driven by CPU to indicate the start of a CPU bus cycle.
HREQ[4:0]#	1.5V	MAIN	I/O GTL+	**Request Command:** HREQ[4:0]# are used to define each transaction type during the clock when ADS# is asserted and the clock after ADS# is asserted.
BREQ0#	1.5V	MAIN	O GTL+	**Symmetric Agent Bus Request:** BREQ0# is driven by the symmetric agent to request for the bus.
BNR#	1.5V	MAIN	I/O GTL+	**Block Next Request:** This signal can be driven asserted by any bus agent to block further requests being pipelined.
HLOCK#	1.5V	MAIN	I GTL+	**Host Lock :** CPU asserts HLOCK# to indicate the current bus cycle is locked.
HIT#	1.5V	MAIN	I/O GTL+	**Keeping a Non-Modified Cache Line:**
HITM#	1.5V	MAIN	I/O GTL+	**Hits a Modified Cache Line:** Hit Modified indicates the snoop cycle hits a modified line in the L1 cache of CPU.
DEFER#	1.5V	MAIN	O GTL+	**Defer Transaction Completion:** SiS630 will use this signal to indicate a retry response to host bus.
RS[2:0]#	1.5V	MAIN	O GTL+	**Response Status:** RS[2:0]# are driven by the response agent to indicate the transaction response type. The following shows the response type. **RS[2:0]** — **Response** 000 — Idle State 100 — Reserved 001 — Retry 101 — No data 010 — Reserved 110 — Implicit Write-back 011 — Reserved 111 — Normal Data
HTRDY#	1.5V	MAIN	I/O GTL+	**Target Ready:** During write cycles, response agent will drive TRDY# to indicate the agent is ready to accept data.
DRDY#	1.5V	MAIN	I/O GTL+	**Data Ready:** DRDY# is driven by the bus owner whenever the data is valid on the bus.
DBSY#	1.5V	MAIN	I/O GTL+	**Data Bus Busy:** Whenever the data is not valid on the bus with DRDY# is deserted, DBSY# is asserted to hold the bus.

Name	Tolerance	Power Plane	Type Attr	Description
BPRI#	1.5V	MAIN	O GTL+	**Priority Agent Bus Request:** BPRI# is driven by the priority agent that wants to request the bus. BPRI# has higher priority than BREQ0# to access a bus.
CPURST#	1.5V	MAIN	O GTL+	**Host Bus Reset:** CPURST# is used to keep all the bus agents in the same initial state before valid cycles issued.
HA[31:3]#	1.5V	MAIN	I/O GTL+	**Host Address Bus :**
HD[63:0]#	1.5V	MAIN	I/O GTL+	**Host Data Bus :**
FERR#	1.5V~5V	MAIN	I	**Floating Point Error :** CPU will assert this signal upon a floating point error occurring.
IGNE#	1.5V~5V	MAIN	OD	**Ignore Numeric Error :** IGNE# is asserted to inform CPU to ignore a numeric error. **Speed Trap for PII :** This pin will be forced to voltage level according to the input value of MD41 or APC0h.4 during system reset period.
NMI	1.5V~5V	MAIN	OD	**Non-Maskable Interrupt :** A rising edge on NMI will trigger a non-maskable interrupt to CPU. Speed Trap for PII : This pin will be forced to voltage level according to the input value of MD44 or APC0h.7 during system reset period.
INTR	1.5V~5V	MAIN	OD	**Interrupt Request :** High-level voltage of this signal indicates the CPU that there is outstanding interrupt(s) needed to be serviced. **Speed Trap for PII :** This pin will be forced to voltage level according to the input value of MD43 or APC0h.6 during system reset period.
CPUSLP#	1.5V~5V	MAIN	OD	**CPU Sleep :** SiS630 can optionally assert CPUSLP# to force the CPU into deep sleep mode when going to S2 state.
STPCLK#	1.5V~5V	MAIN	OD	**Stop Clock :** STPCLK# will be asserted to inhibit or throttle CPU activities upon a pre-defined power management event occurs.
SMI#	1.5V~5V	MAIN	OD	**System Management Interrupt :** SMI# will be asserted when a pre-defined power management event occurs.

5. Pin Descriptions Of Major Components

5.2 SiS630S Slot 1/Socket 370 2D/3D Ultra-AGP™ Single Chipset

Host Bus Interface

Name	Tolerance	Power Plane	Type Attr	Description
INIT#	1.5V~5V	MAIN	OD	**Initialization :** INIT is used to re-start the CPU without flushing its internal caches and registers. In Pentium II platform it is active high. This signal requires an external pull-up resistor tied to 3.3V.
A20M#	1.5V~5V	MAIN	OD	**Address 20 Mask :** When A20M# is asserted, the CPU A20 signal will be forced to "0". **Speed Trap for PII :** This pin will be forced to voltage level according to the input value of MD42 or APC0h.5 during system reset period.

DRAM Controller

Name	Tolerance	Power Plane	Type Attr	Description
SDCLK	3.3V/5V	MAIN	I	SDRAM Clock Input
MD[63:0]	3.3V	MAIN	I/O	System Memory Data Bus
MA[14:0]	3.3V	MAIN	O	System Memory Address Bus
CSA[5:0]#	3.3V	MAIN	O	SDRAM Chip Select
CSB[5:0]#	3.3V	MAIN	O	SDRAM Chip Select Signals (Duplicated Copy)
DQM[7:0]#	3.3V	MAIN	O	SDRAM Input/Output Data Mask
WE#	3.3V	MAIN	O	SDRAM Write Enable
SRAS#	3.3V	MAIN	O	SDRAM Row Address Strobe
SCAS#	3.3V	MAIN	O	SDRAM Column Address Strobe
CKE	3.3V	AUX	O	SDRAM Clock Enable During Suspend-to-DRAM mode (ACPI S2 or S3 state), SDRAM can be put into self-refresh mode by asserting CKE.

PCI Interface

Name	Tolerance	Power Plane	Type Attr	Description
PCICLK	3.3V/5V	MAIN	I	**PCI Clock :** The PCICLK input provides the fundamental timing and the internal operating frequency for the SiS Chip. It runs at the same frequency and skew of the PCI local bus.
C/BE[3:0]#	3.3V/5V	MAIN	I/O	**PCI Bus Command and Byte Enables:** PCI Bus Command and Byte Enables define the PCI command during the address phase of a PCI cycle, and the PCI byte enables during the data phases. C/BE[3:0]# are outputs when the SiS Chip is a PCI bus master and inputs when it is a PCI slave.

Name	Tolerance	Power Plane	Type Attr	Description
AD[31:0]	3.3V/5V	MAIN	I/O	**PCI Address /Data Bus:** In address phase: 1.When the SiS Chip is a PCI bus master, AD[31:0] are output signals. 2.When the SiS Chip is a PCI target, AD[31:0] are input signals. In data phase: 1.When the SiS Chip is a target of a memory read/write cycle, AD[31:0] are floating. 2.When the SiS Chip is a target of a configuration or an I/O cycle, AD[31:0] are output signals in a read cycle, and input signals in a write cycle.
PAR	3.3V/5V	MAIN	I/O	**Parity :** SiS630 drives out Even Parity covering AD[31:0] and C/BE[3:0]#. It does not check the input parity signal.
FRAME#	3.3V/5V	MAIN	I/O	**Frame#:** FRAME# is an output when the SiS Chip is a PCI bus master. The SiS Chip drives FRAME# to indicate the beginning and duration of an access. When the SiS Chip is a PCI slave device, FRAME# is an input signal.
IRDY#	3.3V/5V	MAIN	I/O	**Initiator Ready :** IRDY# is an output when the SiS Chip is a PCI bus master. The assertion of IRDY# indicates the current PCI bus master's ability to complete the current data phase of the transaction. For a read cycle, IRDY# indicates that the PCI bus master is prepared to accept the read data on the following rising edge of the PCI clock. For a write cycle, IRDY# indicates that the bus master has driven valid data on the PCI bus. When the SiS Chip is a PCI slave, IRDY# is an input pin.
TRDY#	3.3V/5V	MAIN	I/O	**Target Ready :** TRDY# is an output when the SiS Chip is a PCI slave. The assertion of TRDY# indicates the target agent's ability to complete the current data phase of the transaction. For a read cycle, TRDY# indicates that the target has driven valid data onto the PCI bus. For a write cycle, TRDY# indicates that the target is prepared to accept data from the PCI bus. When the SiS Chip is a PCI master, it is an input pin.

5. Pin Descriptions Of Major Components

5.2 SiS630S Slot 1/Socket 370 2D/3D Ultra-AGP™ Single Chipset

PCI Interface

Name	Tolerance	Power Plane	Type Attr	Description
STOP#	3.3V/5V	MAIN	I/O	**Stop# :** STOP# indicates that the bus master must start terminating its current PCI bus cycle at the next clock edge and release control of the PCI bus. STOP# is used for disconnection, retry, and target-abortion sequences on the PCI bus.
DEVSEL#	3.3V/5V	MAIN	I/O	**Device Select :** As a PCI target, SiS Chip asserts DEVSEL# by doing positive or subtractive decoding. SiS Chip positively asserts DEVSEL# when the DRAM address is being accessed by a PCI master, PCI configuration registers or embedded controllers' registers are being addressed, or the BIOS memory space is being accessed. The low 16K I/O space and low 16M memory space are responded subtractively. The DEVESEL# is an input pin when SiS Chip is acting as a PCI master. It is asserted by the addressed agent to claim the current transaction.
PLOCK#	3.3V/5V	MAIN	I/O	**PCI Lock :** When PLOCK# is sampled asserted at the beginning of a PCI cycle, SiS630 considers itself being locked and remains in the locked state until PLOCK# is sampled and negated at the following PCI cycle.
PREQ[2:0]#	3.3V/5V	MAIN	I	**PCI Bus Request :** PCI Bus Master Request Signals
PGNT[2:0]#	3.3V	MAIN	O	**PCI Bus Grant :** PCI Bus Master Grant Signals
INT[A:D]#	3.3V/5V	MAIN	I	**PCI interrupt A,B,C,D :** The PCI interrupts will be connected to the inputs of the internal Interrupt controller through the rerouting logic associated with each PCI interrupt.
PCIRST#	3.3V	AUX	O	**PCI Bus Reset :** PCIRST# will be asserted during the period when PWROK is low, and will be kept on asserting until about 24ms after PWROK goes high.
SERR#	3.3V/5V	MAIN	I	**System Error :** When sampled active low, a non-maskable interrupt (NMI) can be generated to CPU if enabled.

PCI IDE Interface

Name	Tolerance	Power Plane	Type Attr	Description
IDA[15:0]	3.3V/5V	MAIN	I/O	Primary Channel Data Bus
IDB[15:0]	3.3V/5V	MAIN	I/O	Secondary Channel Data Bus
IDECSA[1:0]#	3.3V	MAIN	O	Primary Channel CS[1:0]
IDECSB[1:0]#	3.3V	MAIN	O	Secondary Channel CS[1:0]
IIOR[A:B]#	3.3V	MAIN	O	Primary/Secondary Channel IOR# Signals

Name	Tolerance	Power Plane	Type Attr	Description
IIOW[A:B]#	3.3V	MAIN	O	Primary/Secondary Channel IOW# Signals
ICHRDY[A:B]	3.3V/5V	MAIN	I	Primary/Secondary Channel ICHRDY# Signals
IDREQ[A:B]	3.3V/5V	MAIN	I	Primary/Secondary Channel DMA Request Signals
IDACK[A:B]#	3.3V	MAIN	O	Primary/Secondary Channel DMACK# Signals
IIRQ[A:B]	3.3V/5V	MAIN	I	Primary/Secondary Channel Interrupt Signals
IDSAA[2:0]	3.3V	MAIN	O	Primary Channel Address [2:0]
IDSAB[2:0]	3.3V	MAIN	O	Secondary Channel Address [2:0]
CBLID[A:B]	3.3V/5V	MAIN	I	Primary/Secondary Ultra-66 Cable ID

VGA Interface

Name	Tolerance	Power Plane	Type Attr	Description
HSYNC	3.3V	MAIN	O	Horizontal Sync
VSYNC	3.3V	MAIN	O	Vertical Sync
SSYNC	3.3V	MAIN	O	Stereo Sync
DDCCLK	3.3V/5V	MAIN	I/O	Display Data Channel Clock Line
DDCDATA	3.3V/5V	MAIN	I/O	Display Data Channel Data Line
COMP		MAIN	AI	**Compensation Pin:** Connect this pin to AVDD via a 0.1uF capacitor
RSET		MAIN	AI	**Reference Resistor:** An external resistor is connected between the RSET pin and AGND to control the magnitude of the full-scale current.
VREF		MAIN	AI	**Voltage Reference:** Connect 0.1uF Capacitor to Ground.
VCS#	3.3V	MAIN	I/O	VGA Frame Buffer Cache Chip Select
ROUT		MAIN	AO	Red Signal Output
GOUT		MAIN	AO	Green Signal Output
BOUT		MAIN	AO	Blue Signal Output
VBA1 **VBCLK** **PLPWDN#**	3.3V	MAIN	O I/O O	**Display Memory Bank Select:** When 128bits DRAM interface enable, it represents the Memory Bank Select **Digital Video Clock Input:** When Video Bridge connected, it represents the Digital Video Clock Input **Panel Power Down** When external LCD transmitter connected, it represents power down.

5. Pin Descriptions Of Major Components

5.2 SiS630S Slot 1/Socket 370 2D/3D Ultra-AGP™ Single Chipset

VGA Interface

Name	Tolerance	Power Plane	Type Attr	Description
VMA11 **VGCLK**	3.3V	MAIN	O O	**Display Memory Address bit 11 :** When 128bits DRAM interface enable, it represents the Memory Address bit 11 **Digital Video Clock Output:** When Video Bridge connected, it represents the Digital Video Clock Output
VMA10 **VBHCLK**	3.3V	MAIN	O O	**Display Memory Address bit 10:** When 128bits DRAM interface enable, it represents the Memory Address bit 10 **Control Clock Output:** When Video Bridge connected, it represents the Control Clock Output
VMD[63:60]	3.3V	MAIN	I/O	Display Memory Data Bus bits [63:60]
VMD[59:52] **VBRGB[7:0]**	3.3V	MAIN	I/O O	Display Memory Data Bus bits [59:52] Digital Video Data bits [7:0]
VMD[51:49] **VBRGB[18:16]**	3.3V	MAIN	I/O O	Display Memory Data Bus bits [51:49] Digital Video Data bits [18:16]
VMD[48:44] **VBRGB[19:23]**	3.3V	MAIN	I/O O	Display Memory Data Bus bits [48:44] Digital Video Data bits [19:23]
VMD[43:42] **VBRGB[10:11]**	3.3V	MAIN	I/O O	Display Memory Data Bus bits [43:42] Digital Video Data bits [10:11]
VMD[41:40] **VBRGB[9:8]]**	3.3V	MAIN	I/O O	Display Memory Data Bus bits [41:40] Digital Video Data bits [9:8]
VMD[39:38] **VBRGB[13:12]**	3.3V	MAIN	I/O O	Display Memory Data Bus bits [39:38] Digital Video Data bits [13:12]
VMD[37:36] **VBRGB[14:15]**	3.3V	MAIN	I/O O	Display Memory Data Bus bits [37:36] Digital Video Data bits [14:15]
VMD35 **VBBLANKN**	3.3V	MAIN	I/O O	Display Memory Data Bus bit 35 Digital Video Display Enable
VMD[34:33] **TVCTL[0:1]**	3.3V	MAIN	I/O O	Display Memory Data Bus bits [34:33] Video Bridge Data Control bits [0:1]
VMD32 **VBCAD**	3.3V	MAIN	I/O I/O	Display Memory Data Bus bit 32 Video Bridge Programming Control
VMD31 **VBHSYNC**	3.3V	MAIN	I/O I/O	Display Memory Data Bus bit 31 Digital Video Horizontal Sync
VMD30 **VBVSYNC**	3.3V	MAIN	I/O I/O	Display Memory Data Bus bit 30 Digital Video Vertical Sync
VMD29 **DDC2CLK**	3.3V	MAIN	I/O I/O	Display Memory Data Bus bit 29 Second Display data channel clock line
VMD28 **DDC2DATA**	3.3V	MAIN	I/O I/O	Display Memory Data Bus bit 28 Second Display data channel data line
VMD[27:0]	3.3V	MAIN	I/O	Display Memory Data Bus bits [27:0]

Name	Tolerance	Power Plane	Type Attr	Description
VDQM[7:0]	3.3V	MAIN	O	Display Memory SDRAM Input /Output Mask
OSCI	3.3V/5V	MAIN	I	External 14.318MHz Clock Input
ENTEST	3.3V/5V	MAIN	I	Test Mode Enable

Power management Interface

Name	Tolerance	Power Plane	Type Attr	Description
ACPILED	<=5V	AUX	OD	**ACPILED :** ACPILED can be used to control the blinking of an LED at the frequency of 1 Hz to indicate the system is at power saving mode.
EXTSMI#	3.3V/5V	MAIN	I	**External SMI#:** EXTSMI# can be used to generate wakeup event, sleep event, or SCI/SMI#/GPEIRQ event to the ACPI-compatible power management unit.
PME#	3.3V/5V	AUX	I/O	**PME# :** When the system is in power-down mode, an active low event on PME# will cause the PSON# to go low and hence turn on the power supply. When the system is in suspend mode, an active PME# event will cause the system wakeup and generate an SCI/SMI#/GPEIRQ.
PSON#	<=5V	AUX	OD	**ATX Power ON/OFF control:** PSON# is used to control the on/off state of the ATX power supply. When the ATX power supply is in the OFF state, an activated power-on event will force the power supply to ON state.
PWRBTN#	3.3V/5V	AUX	I	**Power Button:** This signal is from the power button switch and will be monitored by the ACPI- mpatible power management unit to switch the system between working and sleeping states.
RING	3.3V/5V	AUX	I	**Ring Indication :** An active RING pulse and lasting for more than 4ms will cause a wakeup event for system to wake from S1~S5.

5. Pin Descriptions Of Major Components

5.2 SiS630S Slot 1/Socket 370 2D/3D Ultra-AGP™ Single Chipset

Power management Interface

Name	Tolerance	Power Plane	Type Attr	Description
THERM#	3.3V/5V	MAIN	I	**Thermal Detect :** THERM# is connected to the internal ACPI-compatible power management unit as an indication of outstanding thermal event. An active THERM# event can be used to generate SCI/SMI#/GPEIRQ. If THERM# is activated for more than 2 second, a thermal override event will occur and the system will enter CPU thermal throttling mode automatically.
GPIO[6:4]	3.3V/5V	AUX	I/O/OD	General Purpose Input/Output [6:4]: Refer to GPIO description.

SMBus Interface

Name	Tolerance	Power Plane	Type Attr	Description
SMBDAT I2CDAT	3.3V/5V	MAIN	I/OD I/OD	**SMBus Data :** SMBus data input/output pin. **I2C Data :** I2C data input/output pin.
SMCLK I2CCLK	3.3V/5V	MAIN	I/OD I/OD	**SMBus Clock :** SMBus clock input/output pin. **I2C Clock :** I2C clock input/output pin.
SMBALT# I2CALT# GPIO15	3.3V/5V	AUX	I/OD I/OD I/O/OD	**SMBus Alert :** This pin is used for SMBus device to wake up the system from sleep state or to generate SCI/SMI#/GPEIRQ. **I2C Alert :** This pin is used for I2C device to wake up the system from sleep state or to generate SCI/SMI#/GPEIRQ. **General Purpose Input/Output 15 :** Refer to GPIO description.

Keyboard controller Interface

Name	Tolerance	Power Plane	Type Attr	Description
KBDAT GPIO10	3.3V/5V	AUX	I/OD I/O/OD	**Keyboard Dada :** When the internal keyboard controller is enabled, this pin is used as the keyboard data signal. **General Purpose Input/Output 10 :** Refer to GPIO description.
KBCLK GPIO11	3.3V/5V	AUX	I/OD I/O/OD	**Keyboard Clock :** When the internal keyboard controller is enabled, this pin is used as the keyboard clock signal. General Purpose Input/Output 11 : Refer to GPIO description.

Name	Tolerance	Power Plane	Type Attr	Description
PMDAT GPIO12	3.3V/5V	AUX	I/OD I/O/OD	**PS2 Mouse Data:** When the internal keyboard and PS2 mouse controllers are enabled, this pin is used as PS2 mouse data signal. **General Purpose Input/Output 12 :** Refer to GPIO description.
PMCLK GPIO13	3.3V/5V	AUX	I/OD I/O/OD	**PS2 Mouse Clock:** When the internal keyboard and PS2 mouse controllers are enabled, this pin is used as the PS2 mouse clock signal. **General Purpose Input/Output 13 :** Refer to GPIO description.
KLOCK# GPIO14	3.3V/5V	AUX	I I/O/OD	**Keyboard Lock:** When KLOCK# is tied low, the internal keyboard controller will not respond to any key-strikes. **General Purpose Input/Output 14 :** Refer to GPIO description.

LPC Interface

Name	Tolerance	Power Plane	Type Attr	Description
LAD[3:0]	3.3V/5V	MAIN	I/O	**LPC Address/Data Bus :** LPC controller drives these four pins to transmit LPC command, address, and data to LPC device.
LDRQ#	3.3V/5V	MAIN	I	**LPC DMA Request 0:** This pin is used by LPC device to request DMA cycle.
LFRAME#	3.3V	MAIN	O	**LPC Frame :** This pin is used to notify LPC device that a start or a abort LPC cycle will occur.
SIRQ	3.3V/5V	MAIN	I/OD	**Serial IRQ :** This signal is used as the serial IRQ line signal.

5. Pin Descriptions Of Major Components

5.2 SiS630S Slot 1/Socket 370 2D/3D Ultra-AGP™ Single Chipset

RTC Interface

Name	Tolerance	Power Plane	Type Attr	Description
AUXOK	1.8V	RTC	I	**Auxiliary Power OK :** This signal is supplied from the power source of resume well. It is also used to reset the logic in resume power well. If there is no auxiliary power source on the system, this pin should be tied together with PWROK.
BATOK	1.8V	RTC	I	**Battery Power OK:** When the internal RTC is enabled, this signal is used to indicate that the power of RTC well is stable. It is also used to reset the logic in RTC well. If the internal RTC is disabled, this pin should be tied low.
OSC32KHI	1.8V	RTC	I	**RTC 32.768 KHz Input** : When internal RTC is enabled, this pin provides the 32.768 KHz clock signal from external crystal or oscillator.
OSC32KHO	<1.8V	RTC	O	**RTC 32.768 KHz Output :** When internal RTC is enabled, this pin should be connected with the other end of the 32.768 KHz crystal or left unconnected if an oscillator is used.
PWROK	1.8V	RTC	I	**Main Power OK** : A high-level input to this signal indicates the power being supplied to the system is in stable operating state. During the period of PWROK being low, CPURST and PCIRST# will all be asserted until after PWROK goes high for 24 ms.

AC'97 interface

Name	Tolerance	Power Plane	Type Attr	Description
AC_BITCLK	3.3V/5V	MAIN	I	**AC'97Bit Clock :** This signal is a 12.288MHz serial data clock, which is generated by primary Codec.
AC_RESET#	3.3V	AUX	O	**AC'97 Reset :** Hardware reset signal for external Codecs.
AC_SDIN[1:0]	3.3V/5V	AUX	I	**AC'97 Serial Data input :** Serial data input from primary Codec and secondary Codec.
AC_SDOUT	3.3V	MAIN	O	**AC'97 Serial Data output :** Serial data output to Codecs.
AC_SYNC	3.3V	MAIN	O	**AC'97 Syncronization :** This is a 48KHz signal, which is used to syncronize the Codecs.
SPDIF **GPIO7**	3.3V/5V	MAIN	O I/O/OD	**S/PDIF Transmitter Output** **General Purpose Input/Output 7 :** Refer to GPIO description.

Fast Ethernet and Homenetworking interface

Name	Tolerance	Power Plane	Type Attr	Description
EECS	3.3V	AUX	O	**Serial EEPROM Chip Select :** This enables the EEPROM during loading of the Ethernet configuration data.
EEDI	3.3V	AUX	O	**Serial EEPROM Data Input :** During serial EEPROM access cycle, the SiS630 will use this pin to serially write OP codes, addresses and data into the serial EEPROM.
EEDO **GPIO3**	3.3V/5V	AUX	I I/O/OD	**Serial EEPROM Data Output :** During serial EEPROM access cycle, the SiS630 will read the contents of the EEPROM serially through this pin. Requires external pull-up resistor. **General Purpose Input/Output 3 :** Refer to GPIO description.
EESK	3.3V	AUX	O	**Serial EEPROM Clock :** This pin provides the clock for the serial EEPROM.
OSC25MHI	3.3V	AUX	I	**PHY 25MHz Clock Input :** This pin is supplied the 25MHz clock signal input from the external crystal or an oscillator.
PLEDO# **OC3#** **GPIO8**	3.3V	AUX	OD O I/O/OD	**Programmable LED Output :** (A)Select 10/100Mbps LAN Mode: This pin is used as an LINK/ACTIVITY indication output. (B)Select Home Networking Mode: This pin is also an LINK/ACTIVITY indication output. **OC3# :** When this pin is configured as OC3#, it can detects USB Port 3 over current condition. **General Purpose Input/Output 8 :** Refer to GPIO description.
REXT		AUX	I	**Transmit Current Set :** An external resistor connected between this pin and GND will set the output current level for the twisted pair outputs.
TPIP		AUX	I	Twisted Pair Receive Positive Input
TPIN		AUX	I	Twisted Pair Receive Negative Input
TPOP		AUX	O	Twisted Pair Transmit Positive Output
TPON		AUX	O	Twisted Pair Transmit Negative Output
HRTXRXP		AUX	I/O	Twisted Pair Transmit / Receive Positive Data
HRTXRXN		AUX	I/O	Twisted Pair Transmit / Receive Negative Data

5. Pin Descriptions Of Major Components

5.2 SiS630S Slot 1/Socket 370 2D/3D Ultra-AGP™ Single Chipset

USB interface

Name	Tolerance	Power Plane	Type Attr	Description
CLK48M	3.3V/5V	MAIN	I	**USB 48 MHz clock input :** This signal provides the fundamental clock for the USB Controller.
OC0# **PCIREQ3#** **GPIO0**	3.3V/5V	MAIN	I I I/O/OD	**USB Port 0 Over Current Detection :** OC0# is used to detect the over current condition of USB Port 0. **External PCI Master Request 3:** PCIREQ3# is used for PCI Device on PCI Slot 3 to assert its request to hold PCI Bus. **General Purpose Input/Output 0 :** Refer to GPIO description.
OC1# **PCIGNT3#** **GPIO1**	3.3V/5V	MAIN	I O I/O/OD	**USB Port 1 Over Current Detection :** OC1# is used to detect the over current condition of USB Port 1. **External PCI Master Grant 3 :** PCIGNT3# is used to indicate PCI Device on PCI Slot 3 the PCI Bus has been granted. **General Purpose Input/Output 1 :** Refer to GPIO description.
OC3# **LDRQ1#** **GPIO2**	3.3V/5V	MAIN	I I I/O/OD	**USB Port 3 Over Current Detection:** OC3# is used to detect the over current condition of USB Port 3. **LPC DMA Request 1 :** LDRQ1# is the second LPC DMA request signal used by LPC Device to request DMA cycles. **General Purpose Input/Output 2 :** Refer to GPIO description.
USBP[4:0]P	3.3V	AUX	I/O	USB Port [4:0] Positive Input/Output
USBP[4:0]N	3.3V	AUX	I/O	USB Port [4:0] Negative Input/Output

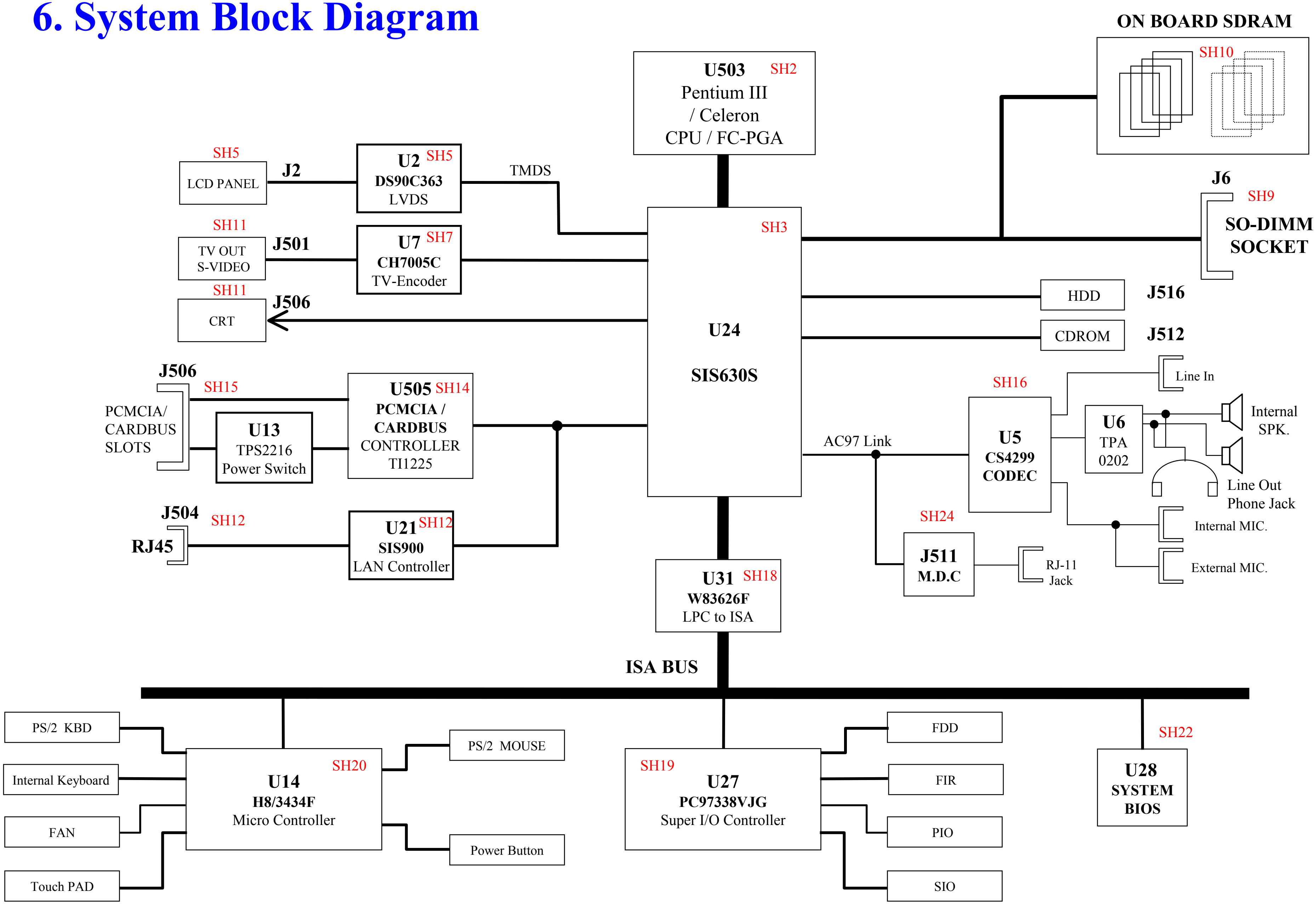
Legacy I/o and Miscellaneous Signals

Name	Tolerance	Power Plane	Type Attr	Description
SPK	3.3V	MAIN	O	**Speaker output :** The SPK is connected to the system speaker.

Power and Ground Signals

Name	Tolerance	Power Plane	Type Attr	Description
VSS		GROUND		0V
IVDD		MAIN		1.8V
IVDD (AUX)		AUX		1.8V
OVDD (AUX)		AUX		3.3V
USBVDD		AUX		3.3V
RTCVDD		RTC		1.8V
DCLKAVDD		MAIN		3.3V
ECLKAVDD		MAIN		3.3V
TXAVDD		AUX		3.3V
RXAVDD		AUX		3.3V
DACAVDD		MAIN		3.3V
IDEAVDD		MAIN		1.8V
SDAVDD		MAIN		3.3V
CPUAVDD		MAIN		3.3V
VTTB		MAIN		1.5V
VSSQ		GROUND		0V
VTTA		MAIN		1.5V
VCC3		MAIN		3.3V

6. System Block Diagram



7. Maintenance Diagnostics

7.1 Introduction

Each time the computer is turned on, the system bios runs a series of internal checks on the hardware. This power-on self test (post) allows the computer to detect problems as early as the power-on stage. Error messages of post can alert you to the problems of your computer.

If an error is detected during these tests, you will see an error message displayed on the screen. If the error occurs before the display is initialized,then the screen cannot display the error message. Error codes or system beeps are used to identify a post error that occurs when the screen is not available.

The value for the diagnostic port (378H) is written at the beginning of the test. Therefore, if the test failed, the user can determine where the problem occurred by reading the last value written to port 378H by the 378H port debug board plug at PIO PORT.

7. Maintenance Diagnostics

7.2 Error Codes : Following is a list of error codes in sequent display on the PIO debug board.

SYSTEM SOFT BIOS:

CODE	DESCRIPTION
01h	Start of boot loader sequence.
02h	Initialize chipset.
03h	Memory Sizing.
04h	Perform conventional RAM(1st 640K) test with crossed-pattern R/W
05h	Move boot loader to the RAM.
06h	Start point of execution of boot loader in RAM.
07h	Shadow system BIOS.
08h	Initialize clock synthesizer
09h	Initialize audio controller.
0Ah	Detect internal ISA MODEM
0Bh	Proceed with normal boot
0Ch	Proceed with crisis boot
0Fh	DRAM sizing
10h	Initial L1,L2 cache, make stack and diagnose CMOS.
11h	Turn off fast A20 for post. Reset GDT's, 8259s quickly.
12h	Signal power on reset at COMS.
13h	Initialize the chipset, (SDRAM).
14h	Search for ISA bus VGA adapter
15h	Reset counter/timer 1, exite the RAM.
16h	User register config through CMOS
18h	Dispatch to 1st 64K RAM test
19h	Checksum the ROM
1Ah	Reset PIC's(8259s)
1Bh	Initialize video adapter(s)
1Ch	Initialize video (6845 regs)

CODE	DESCRIPTION
1Dh	Initialize color adapter
1Eh	Initialize monochrome adapter
1Fh	Test 8237A page registers
20h	Perform keyboard self test
21h	Test & initialize keyboard controller
22h	Check if CMOS RAM valid
23h	Test battery fail & CMOS X-SUM
24h	Test the DMA controllers
25h	Initialize 8237A controller
26h	Initialize interrupt vectors table.
27h	RAM quick sizing
28h	Protected mode entered safely
29h	RAM test completed
2Ah	Protected mode exit successful
2Bh	Setup shadow
2Ch	Prepare to initialize video
2Dh	Search for monochrome adapter
2Eh	Search for color adapter, VGA initialize.
2Fh	Signon messages displayed
30h	Special init of keyboard ctlr
31h	Test if keyboard present
32h	Test keyboard interrupt
33h	Test keyboard command Byte
34h	Test, blank and count all RAM
35h	Protected mode entered safely (2).
36h	RAM test complete

7. Maintenance Diagnostics

7.2 Error Codes : Following is a list of error codes in sequent display on the PIO debug board.

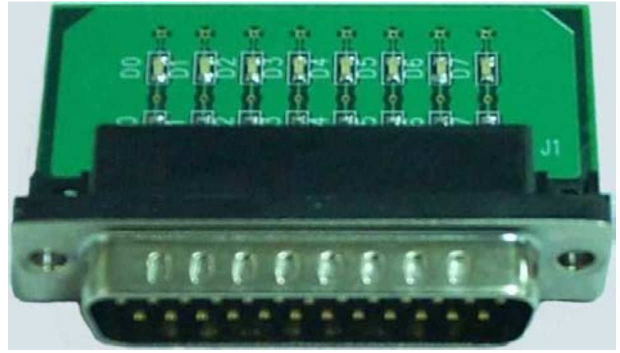
SYSTEM SOFT BIOS:

CODE	DESCRIPTION
37h	Protected mode exit successful
38h	Update keyboard output port to disable gate of A20
39h	Setup cache controller
3Ah	Test if 18.2Hz periodic working
3Bh	Initialize BIOS data area at 40:0.
3Ch	Initialize the hardware interrupt vector tabl
3Dh	Search and init the Mouse
3Eh	Update num lock status
3Fh	OEM initialization of COMM and LPT ports
40h	Configure the COMM and LPT ports
41h	Initialize the floppies
42h	Initialize the hard disk
43h	OEM's init of PM with USB
44h	Initialize additional ROMs
45h	Update NUMLOCK status
46h	Test for coprocessor installed
47h	OEM's init of power management, (check SMI)
48h	OEM functions before boot (PCMCIA, CardBus)
49h	Dispatch to operation system boot
4Ah	Jump into bootstrap code

7. Maintenance Diagnostics

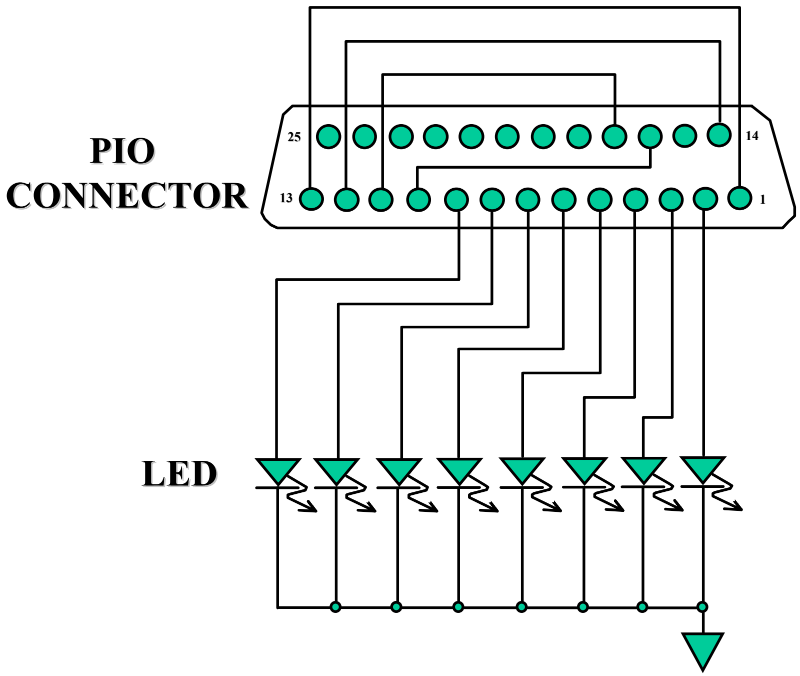
7.3.1 Diagnostic Tools :

- LED * 8 OR
- PIO CONNECTOR * 1



P/N:411904800001
DESCRIPTION :PWA;PWA-378PORT DEBUG BD
Note:Order it from MIC/TSSC

7.3.2 CIRCUIT:



PIN1 : STROBE ⟷ PIN 13 : SLCT

PIN10: ACK# ⟷ PIN 16 : INT#

PIN11: BUSY ⟷ PIN 17 : SELIN#

PIN12: PTERR ⟷ PIN 14 : AUTOFD#

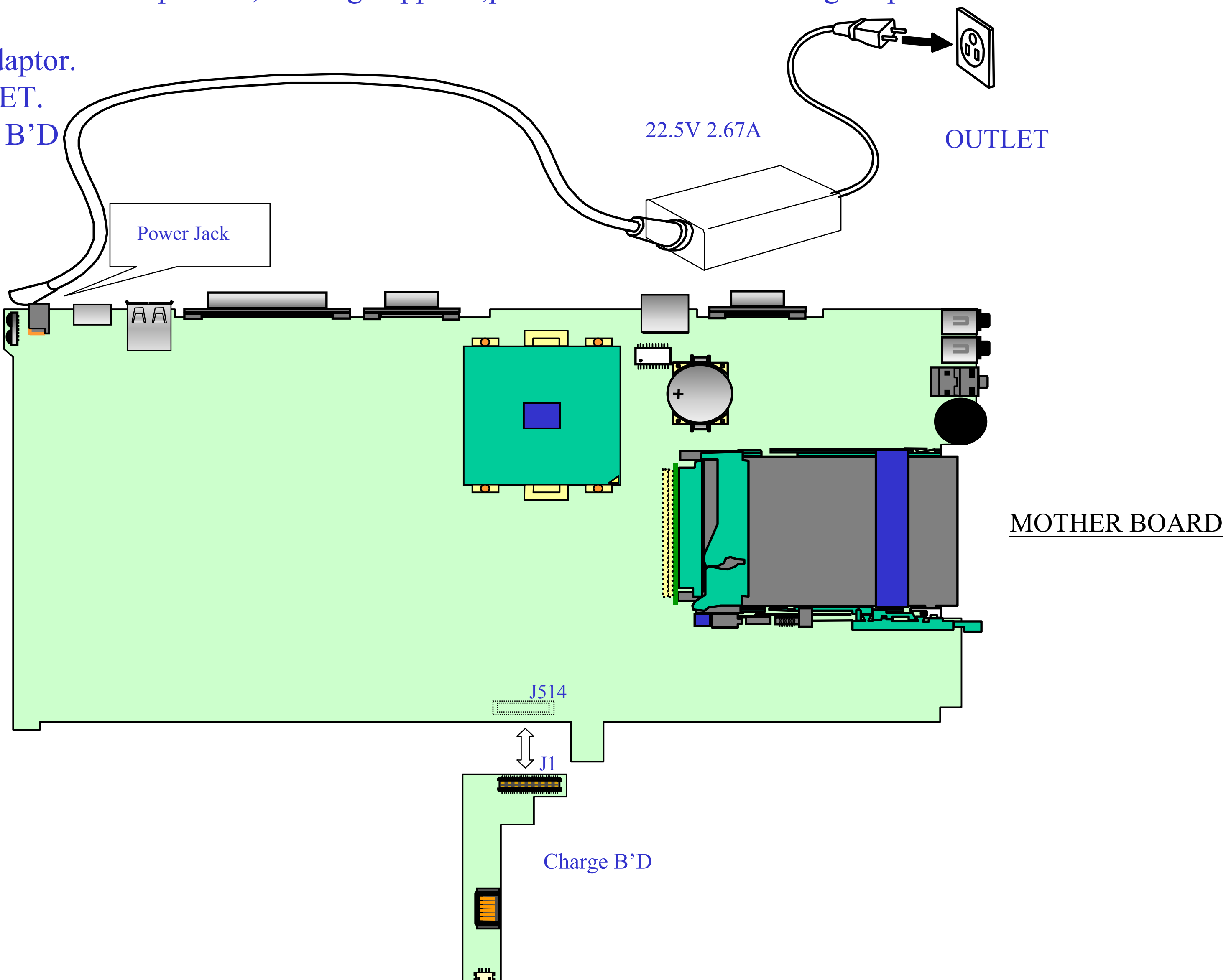
PIN{9:2}: PD{7:0}

8. TROUBLE SHOOTING

8.1 NO POWER:

When the power button is pressed, nothing happens ,power indicator does not light up.

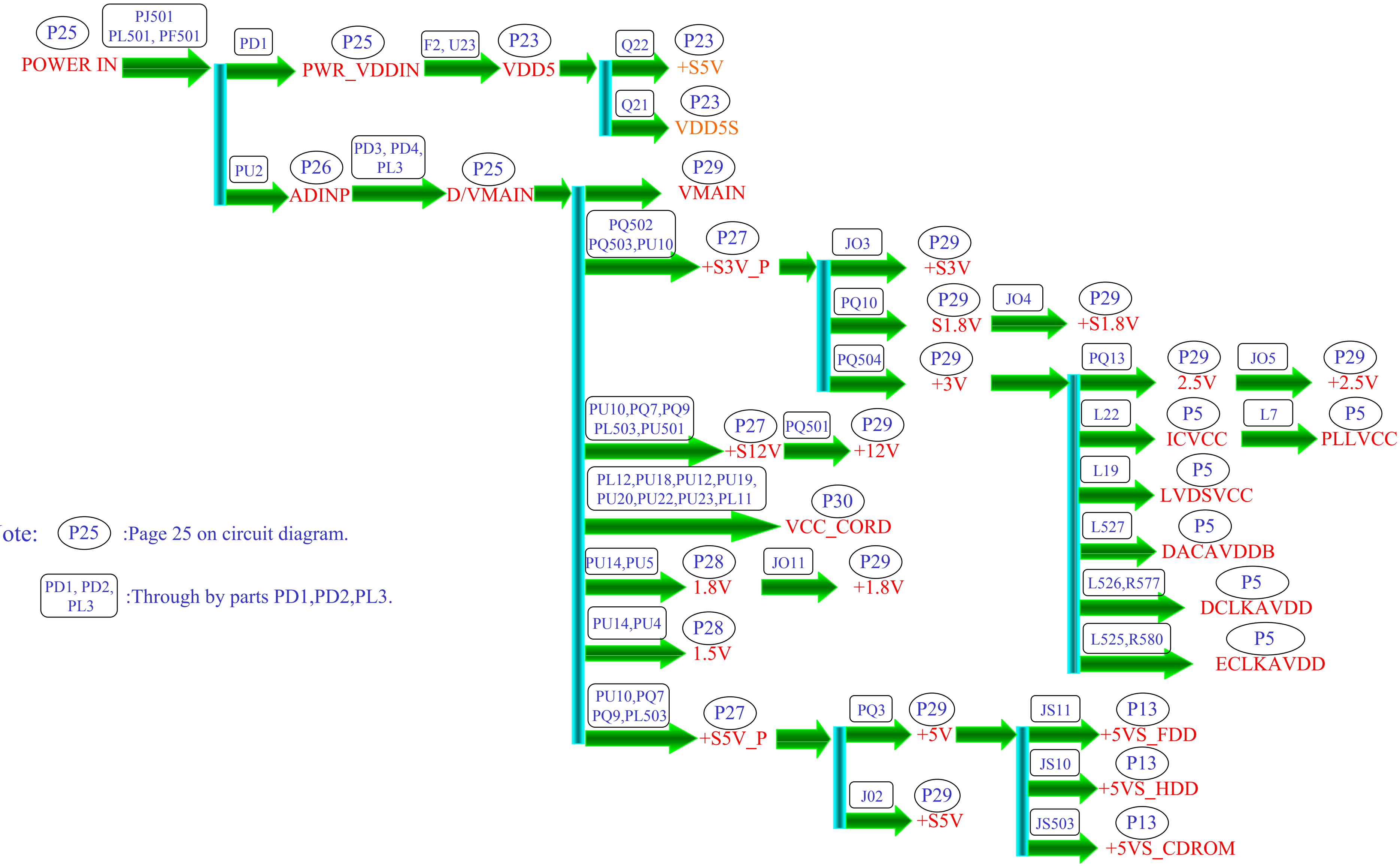
1. Check AC Adaptor.
2. Check OUTLET.
3.Check Charge B'D



7521Plus / N N/B MAINTENANCE

8.1 NO POWER:

When the power button is pressed, nothing happens ,power indicator does not light up.



Note: (P25) :Page 25 on circuit diagram.

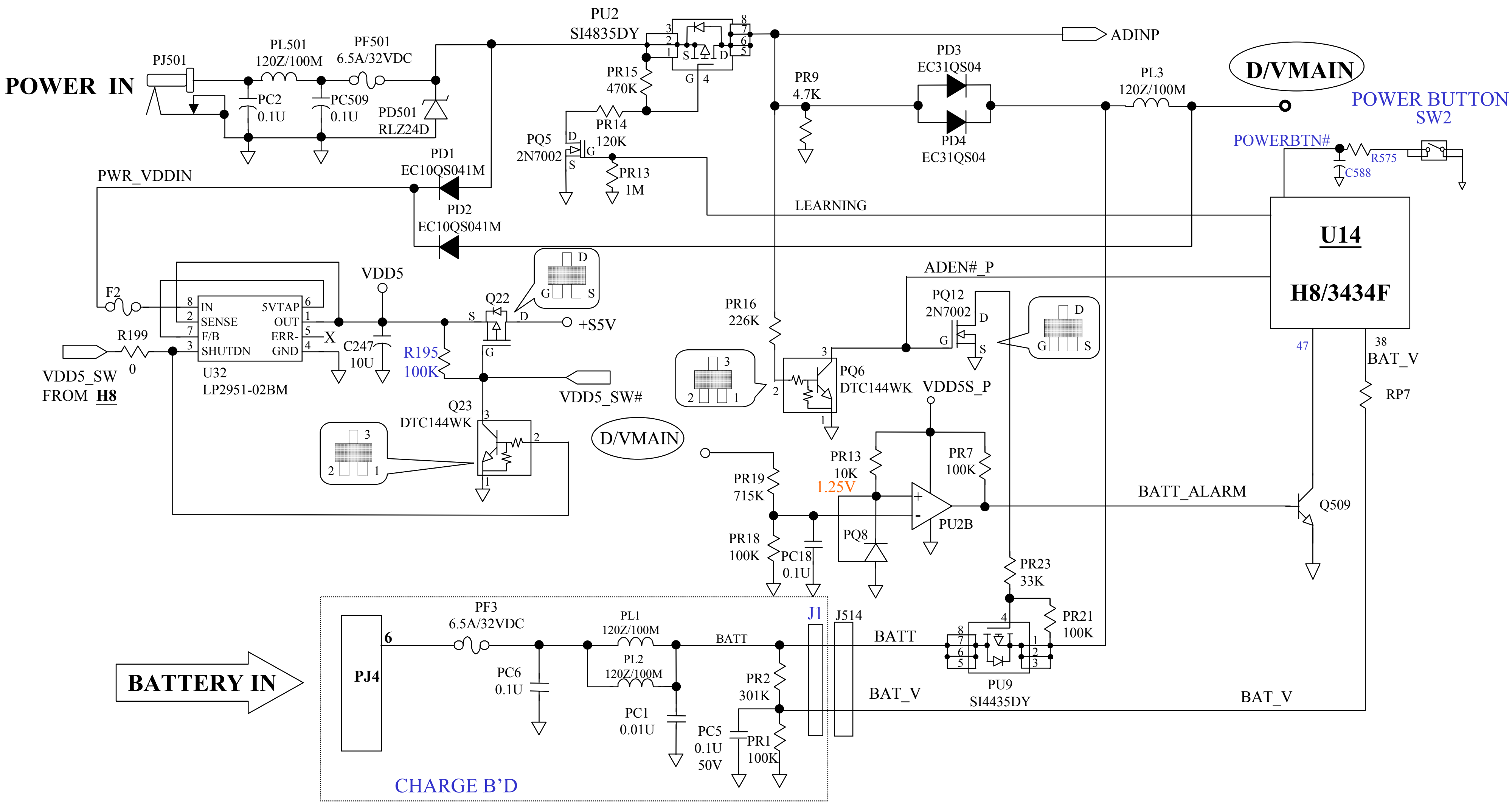
[PD1, PD2, PL3] :Through by parts PD1,PD2,PL3.

7521Plus / N N/B MAINTENANCE

8.1 NO POWER:

Symptom:

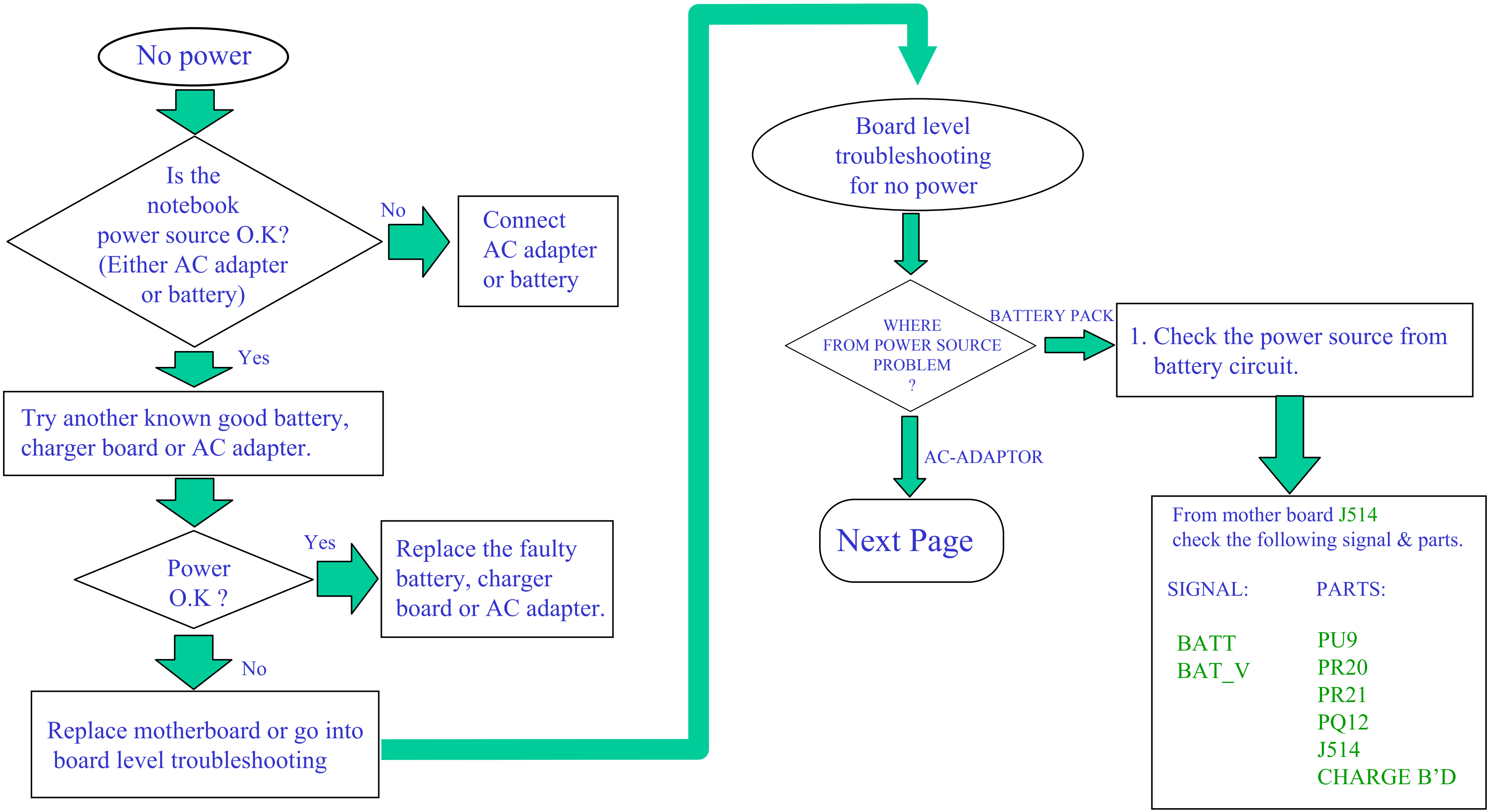
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



8.1 NO POWER:

Symptom:

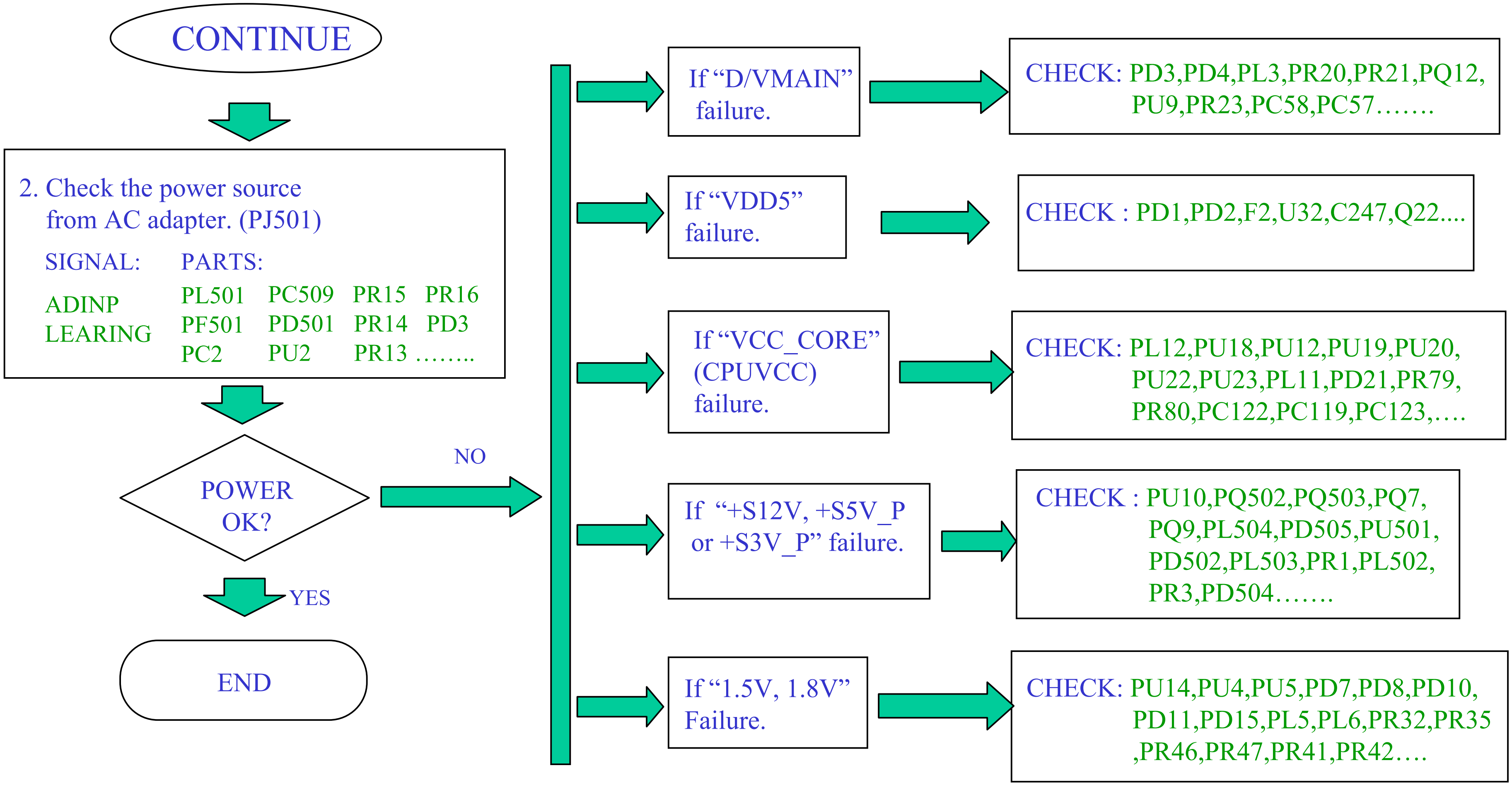
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



8.1 NO POWER:

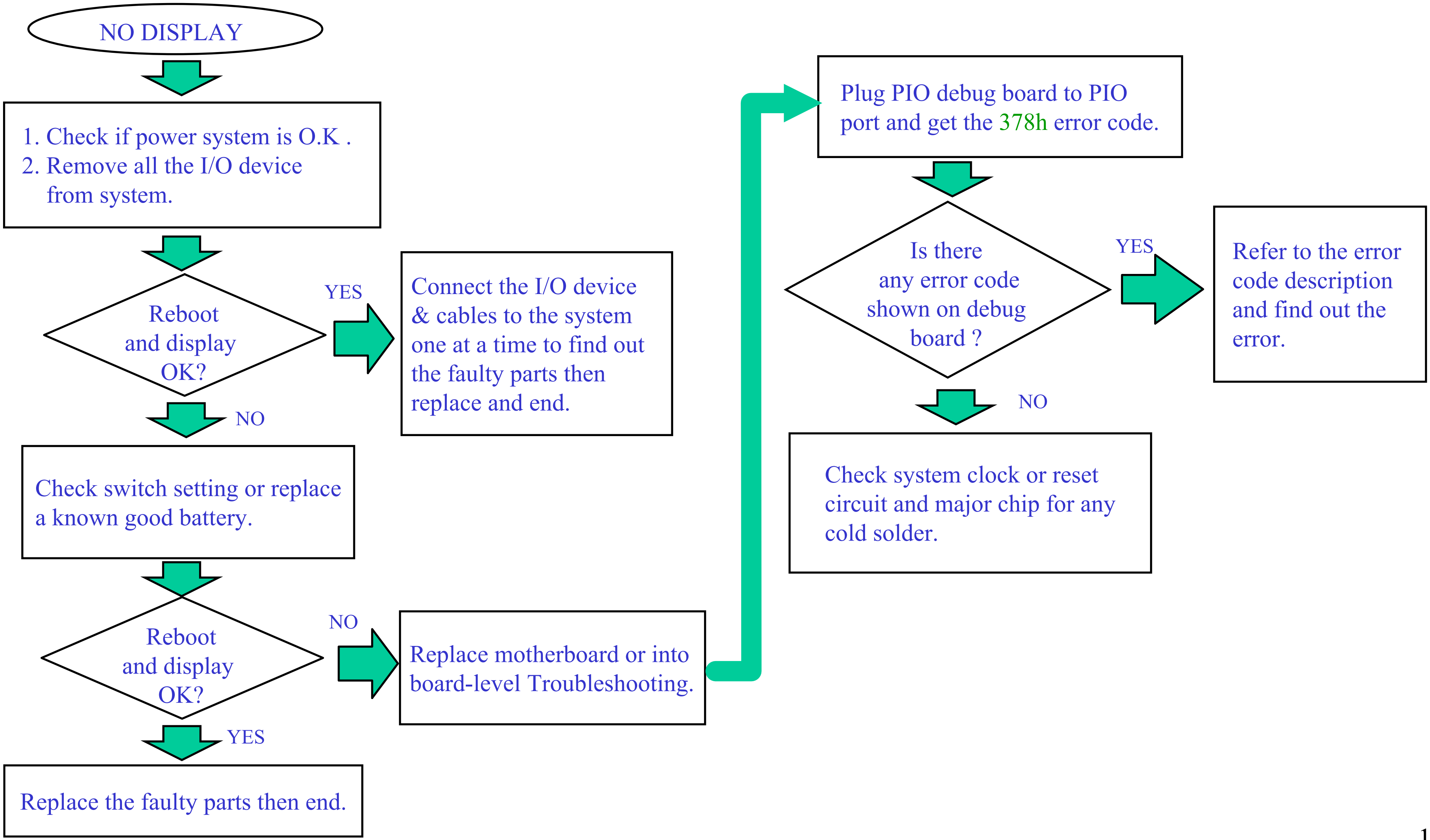
Symptom:

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



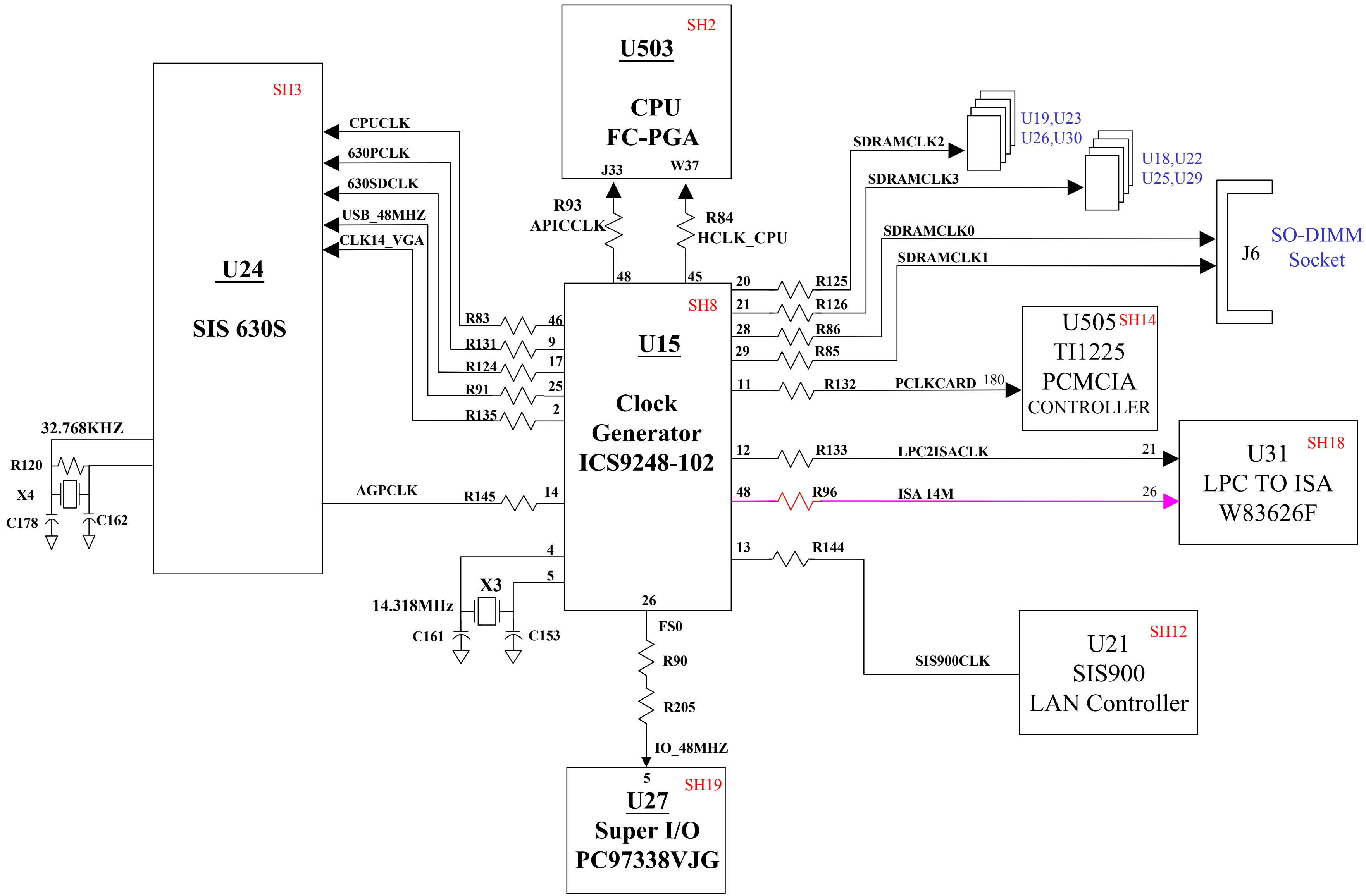
8.2 NO DISPLAY

There is no display on both LCD and monitor



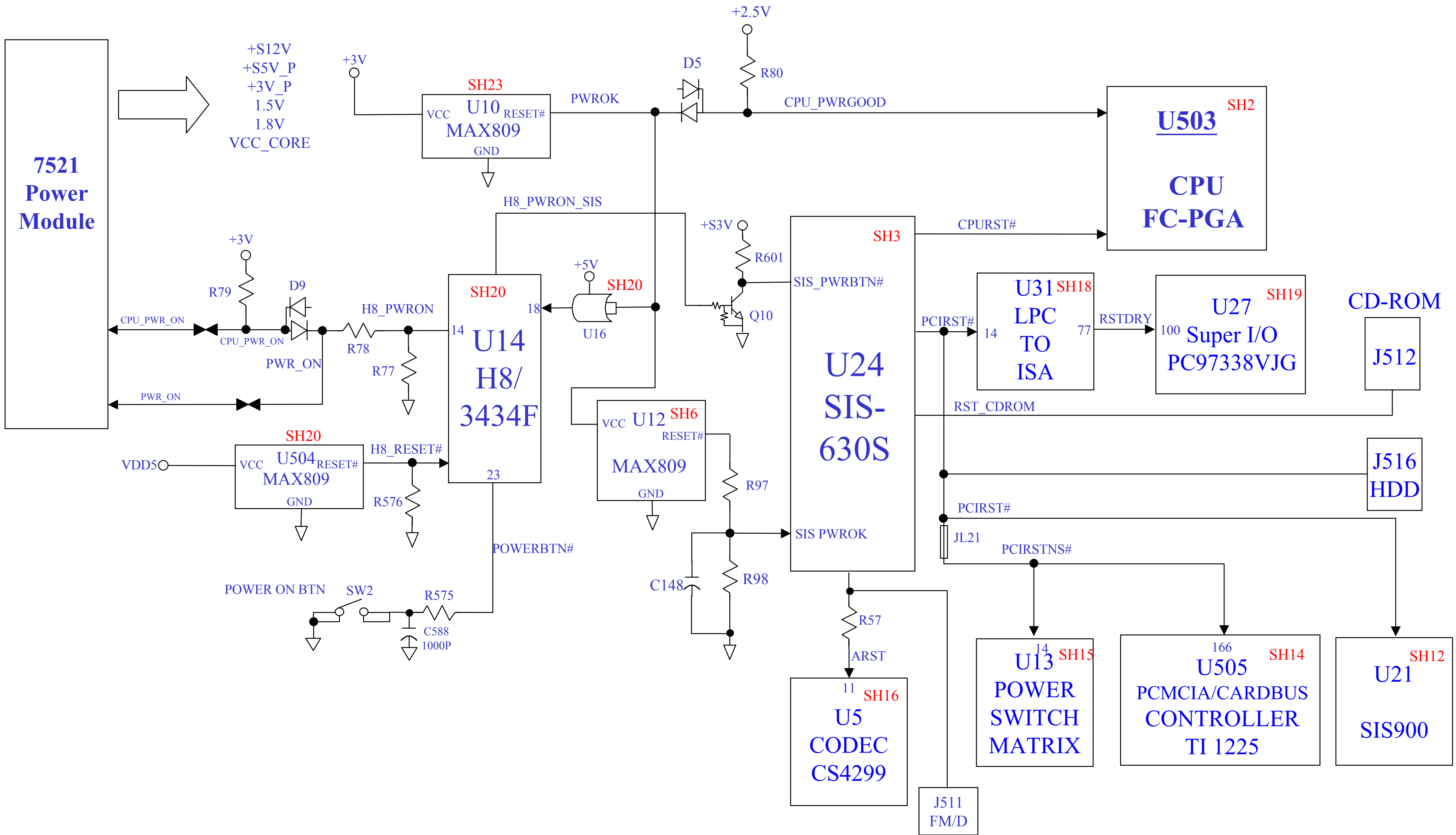
8.2 NO DISPLAY

******System Clock Check ******



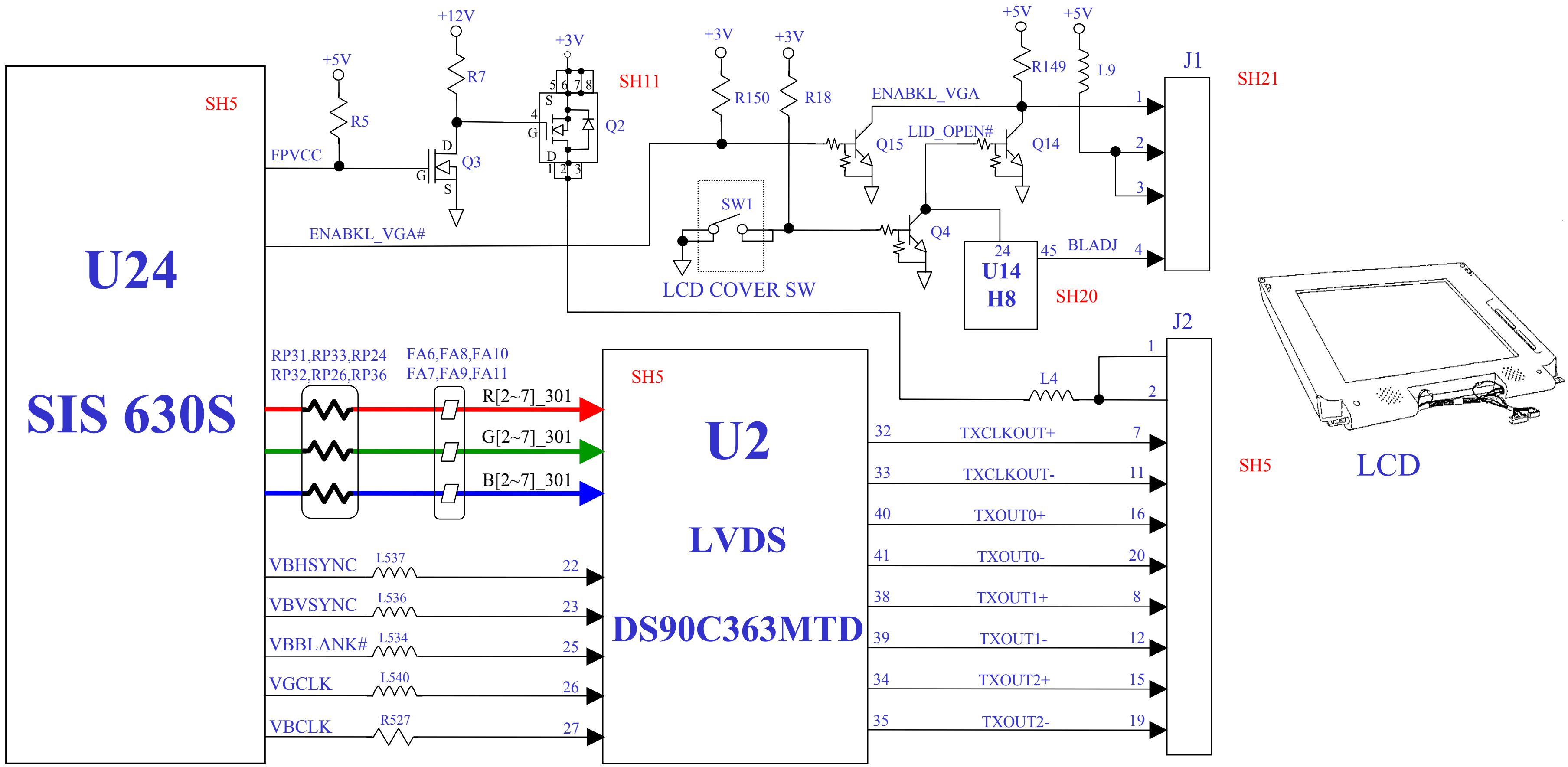
8.2 NO DISPLAY

******Power Good & Reset System ******



8.3 VGA CONTROLLER FAILURE LCD NO DISPLAY

There is no display or picture abnormal on LCD.



8.3 VGA CONTROLLER FAILURE LCD NO DISPLAY

There is no display or picture abnormal on LCD.

VGA CONTROLLER FAILURE

1. Confirm LCD panel or monitor is good and check the cable are connected properly.
2. Try another known good monitor or LCD module.

Display OK?

YES → Replace faulty LCD or monitor.

NO ↓

Remove all the I/O device & cable from motherboard except LCD panel or extended monitor.

Display OK?

YES → Connect the I/O device & cable to the M/B one at a time to find out which part is causing the problem.

NO ↓

Replace motherboard or into board-level Troubleshooting.

Check if U24, U2, J1, J2 are cold solder?

YES → Re-soldering.

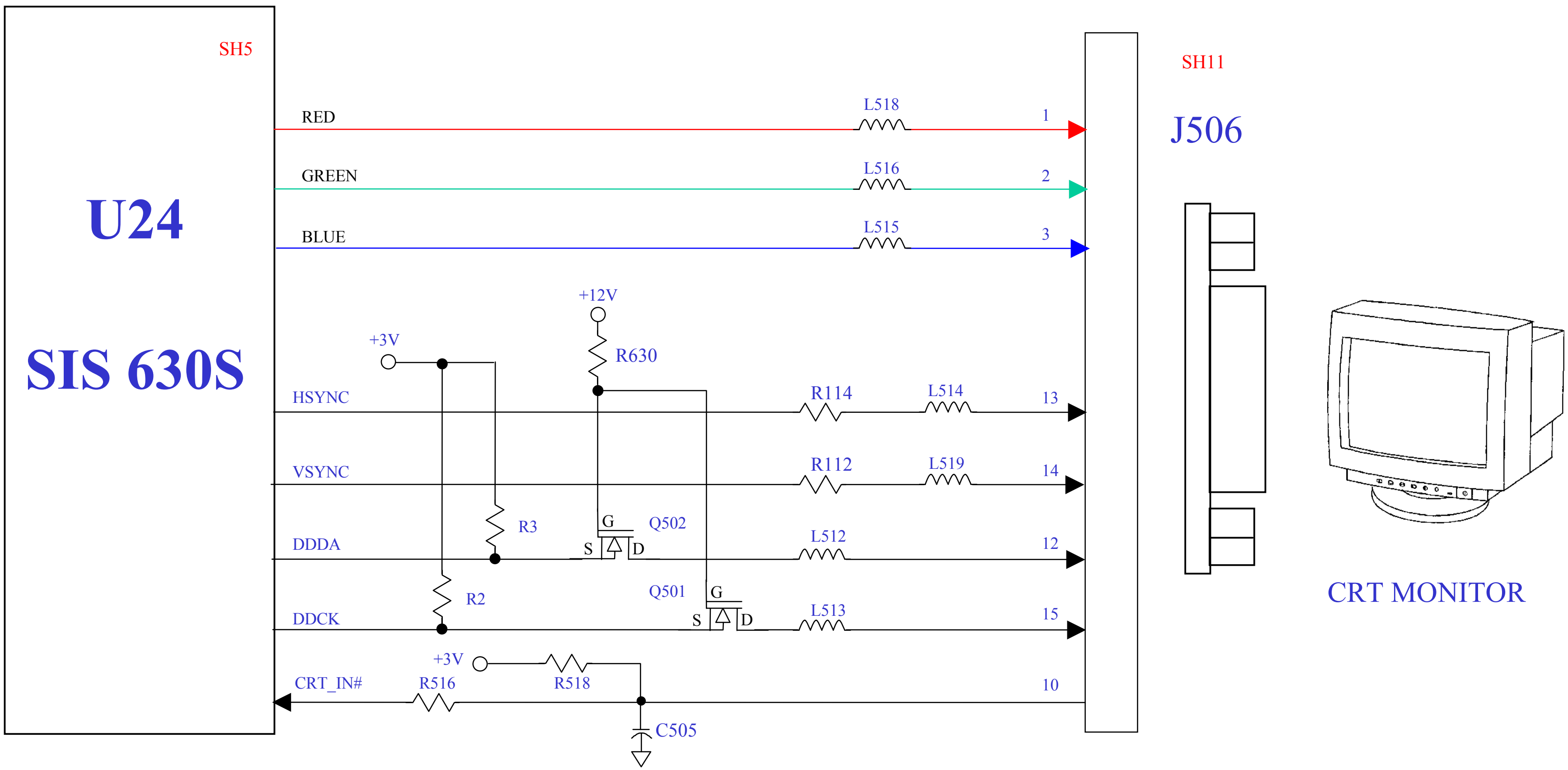
NO ↓

One of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:				Signals:	
U24	U2	FA8	FA9	R[2~7]301	TXCLKOUT-
J1	J2	FA11	FA10	G[2~7]301	TXCLKOUT+
Q2	Q3	FA6	FA7	B[2~7]301	TXOUT0-
Q4	Q15	RP11	RP12	VBHSYNC	TXOUT0+
Q14	U14	RP31	RP33	VBVSYNC	TXOUT1-
SW1	R5	RP24	RP32	VBBLANK#	TXOUT1+
R7	R150	RP26	RP36	VGCLK	TXOUT2-
L9	R18	L540	R527	FPVCC	TXOUT2+
R149	L537			LID_OPEN#	
L536	L534				

8.4 EXTERNAL MONITOR NO DISPLAY

There is no display or picture abnormal on CRT monitor.



8.4 EXTERNAL MONITOR NO DISPLAY

There is no display or picture abnormal on CRT monitor.

VGA CONTROLLER FAILURE

1. Confirm monitor is good and check the cable are connected properly.
2. Try another known good monitor.

Display OK?

YES → Replace faulty monitor.

NO ↓

Remove all the I/O device & cable from motherboard except monitor.

Display OK?

YES → Connect the I/O device & cable to the M/B one at a time to find out which part is causing the problem.

NO ↓

Replace motherboard or into board-level Troubleshooting.

Check if U24, J506 are cold solder?

YES → Re-soldering.

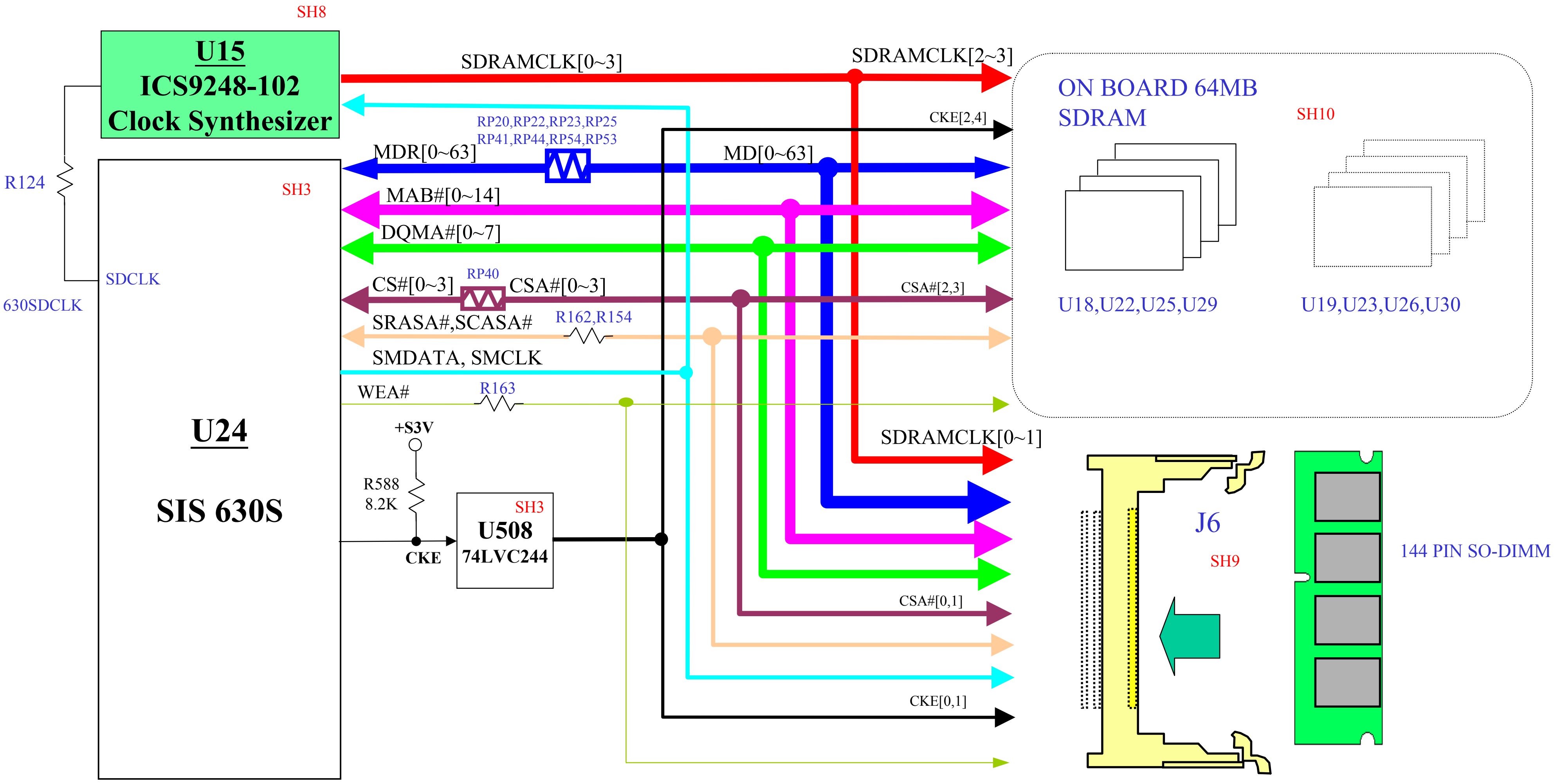
NO ↓

One of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:		Signals:
U24	PR15	CRT_IN#
J506	L514	RED
R114	L519	GREEN
R112	L512	BLUE
C505	L513	HYNC
L518	Q501	VSYNC
L516	Q502	DDCK
L515	R2	DDDA
CA501	R3	
CA502		

8.5 MEMORY TEST ERROR

Either on board or extend SDRAM is failure or system hangs up.



8.5 MEMORY TEST ERROR

Either on board or extend SDRAM is failure or system hangs up.

MEMORY TEST ERROR

1. Check if on board SDRAM chips are no cold solder.
2. Check the extend SDRAM module is installed properly. (J6)
3. Confirm the SDRAM socket is ok, no band pins.

Test OK?

YES → Correct it.

NO ↓

Try another known good SDRAM modules.

Test OK?

YES → END

NO → Replace mother board or into board level Troubleshooting.

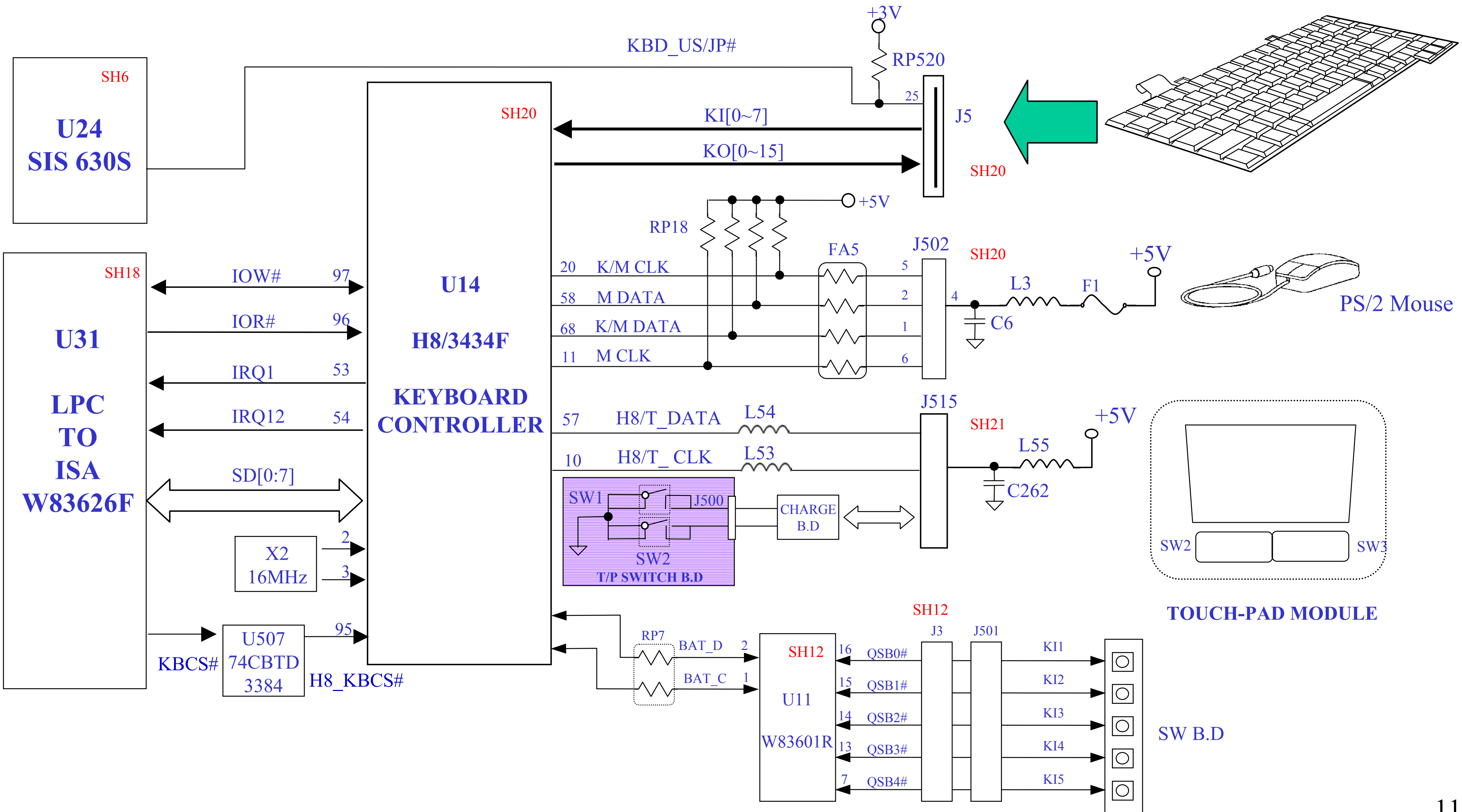
Board-level Troubleshooting for Memory test error.

Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	Signals:	
U24, U15	MDR[0~63]	CSA#[0:3]
U18, U22	MD[0~63]	CKE[0:3]
U25, U29	MAB#[0~9]	SDRAMCLK[0:3]
U19, U23	MAB[10,13]	SMBDATA
U26, U30	MAB#[11,12]	SMBCLK
RP20, RP22	SCASA#,	
RP23, RP25	SRASA#	
RP41, RP44	WEA#	
RP54, RP53	DQMA#[0:7]	
RP40, J6		
R588, U508		

8.6 KEYBOARD(K/B) TOUCH-PAD(T/P) , ESB TEST ERROR

Error message of keyboard failure is shown or any key doesn't work.



8.6 KEYBOARD(K/B) TOUCH-PAD(T/P) , ESB TEST ERROR

Error message of keyboard or touch pad failure is shown or any key doesn't work.

KEYBOARD TEST ERROR

Check if K/B or T/P cable installed properly.

Test OK? YES → Correct it then end.

NO

Try another known good K/B or T/P (Internal or external).

Test OK? YES → Replace the faulty K/B or T/P then end.

NO

Replace M/B or into board-level Troubleshooting

Board-level Troubleshooting for K/B or T/P test error.

Check if U14, J5, J515 and J502 are cold solder or not.

Test OK? YES → Replace or Re-solder U14, J5, J515 and J502

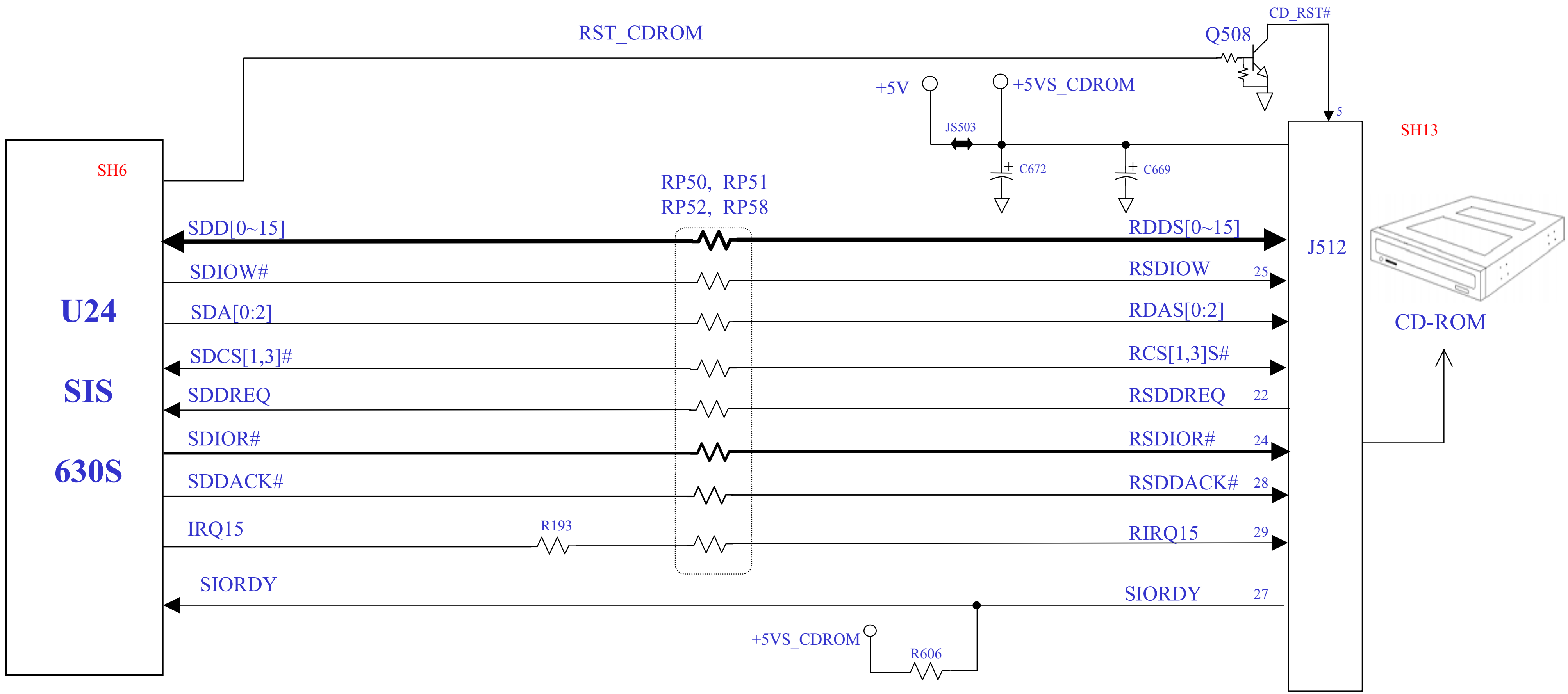
NO

Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:		Signals:	
U14, U31	CHARGE BD	KI[0:7]	IOW#
R520, RP18	SWITCH BD	KO[0:15]	IOR#
FA5, L3		H8/T_DATA	IRQ1
F1, L53		H8/T_CLK	IRQ12
L54, RP7		H8_KBCS#	SD[0:7]
U11, L55			
C262, J3			
J501			

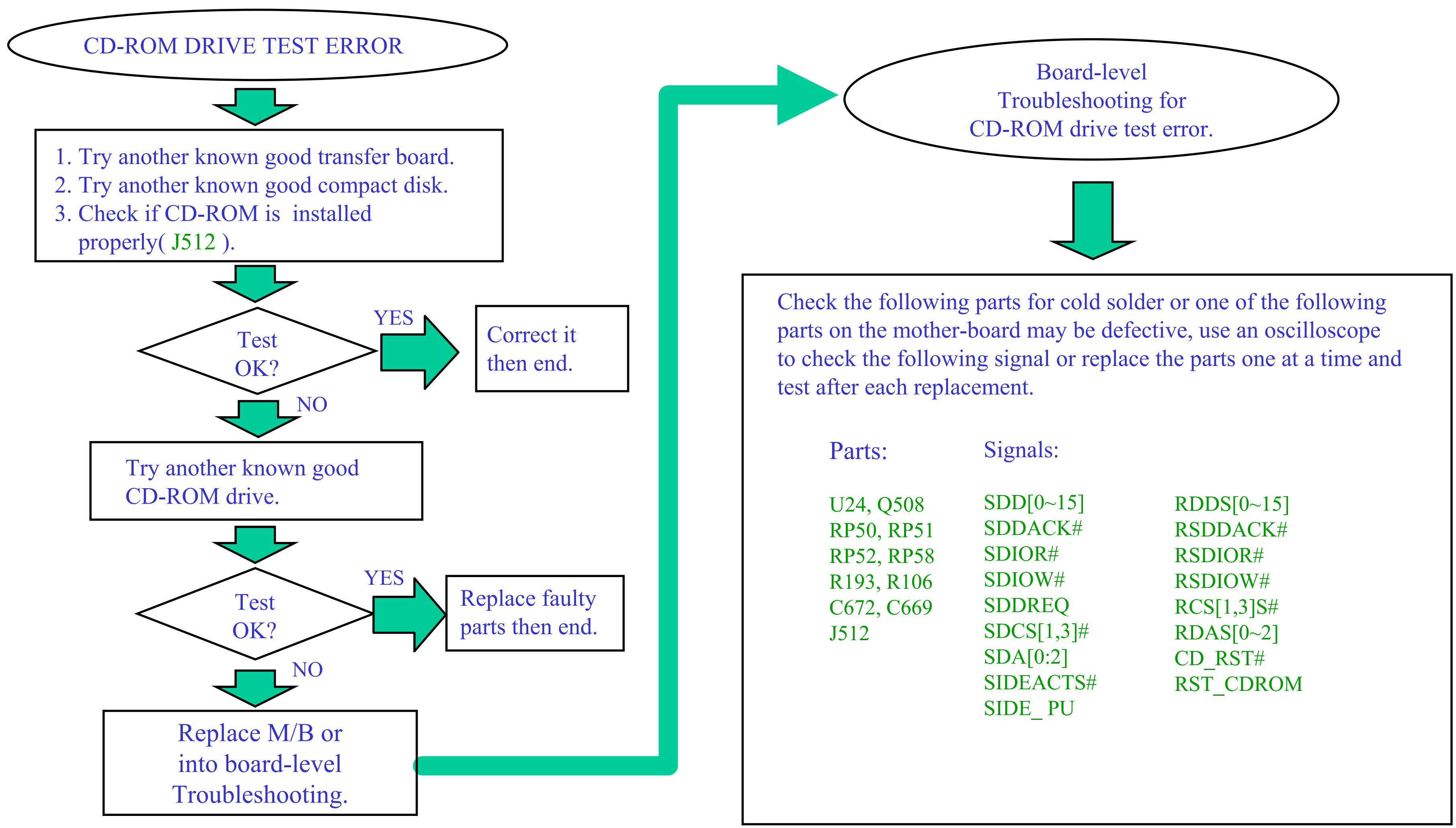
8.7 CD-ROM DRIVE TEST ERROR

An error message is shown when reading data from CD-ROM drive.



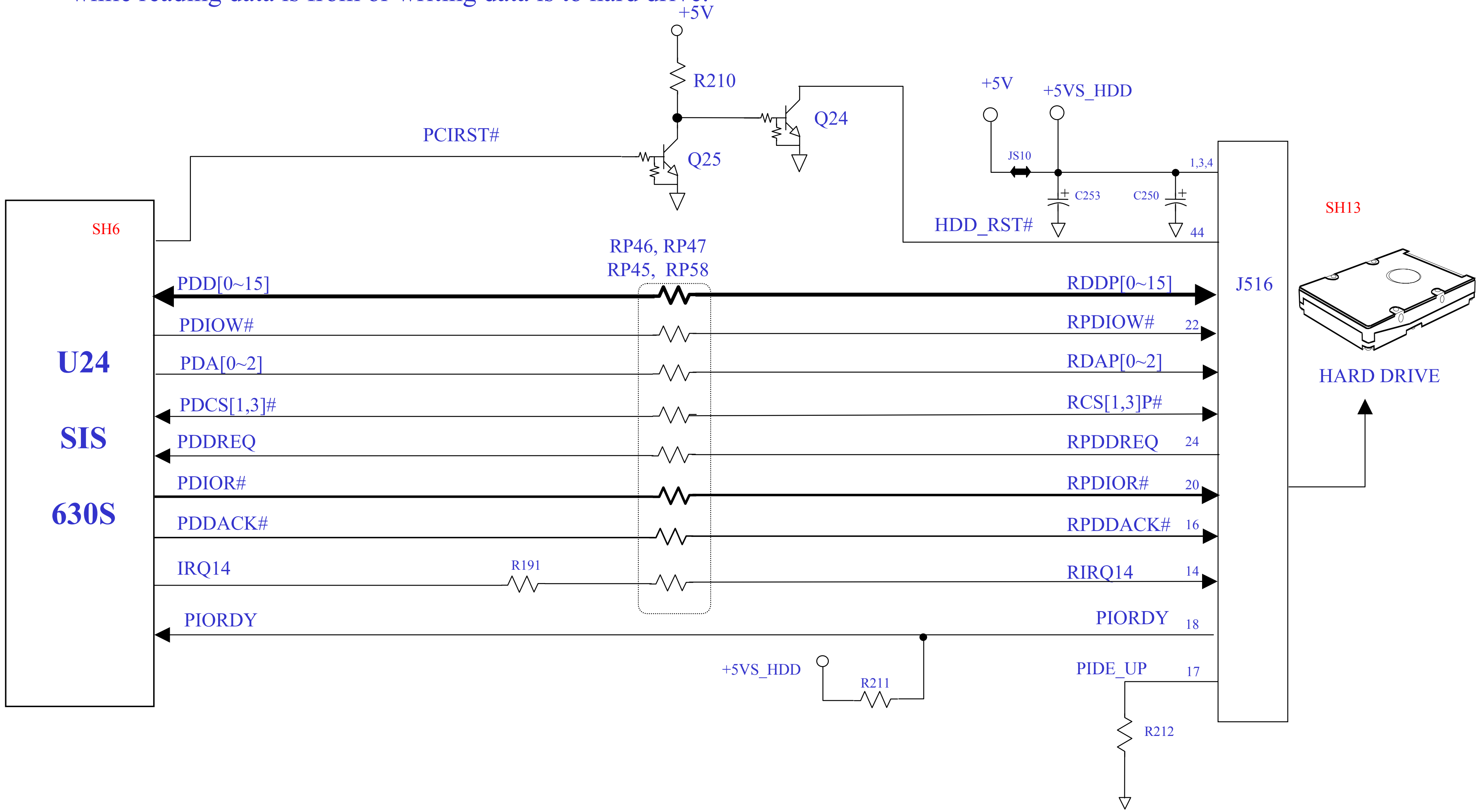
8.7 CD-ROM DRIVE TEST ERROR

An error message is shown when reading data from CD-ROM drive.



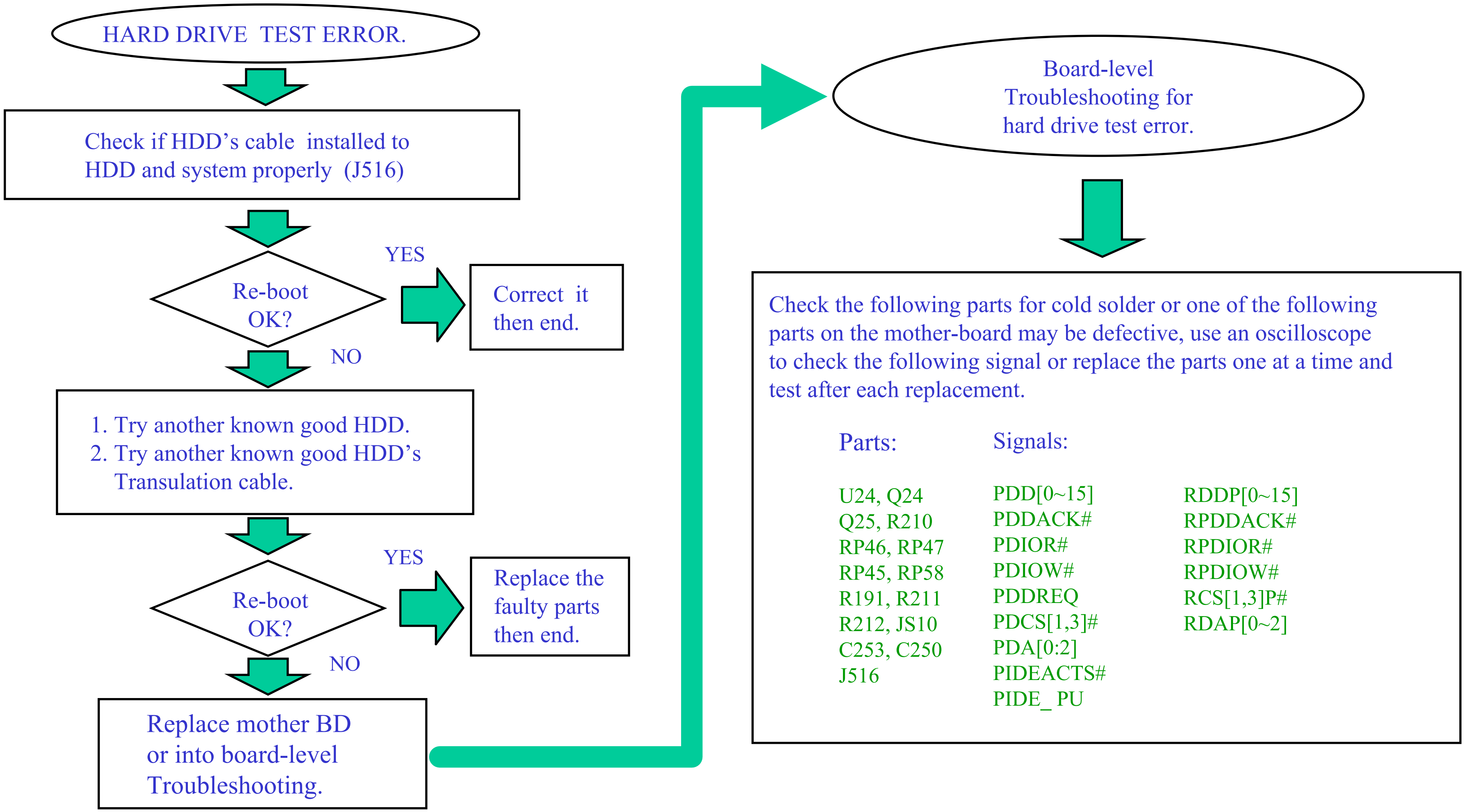
8.8 HARD DRIVE TEST ERROR

Either an error message is shown , or the driver motor continues spinning , while reading data is from or writing data is to hard drive.



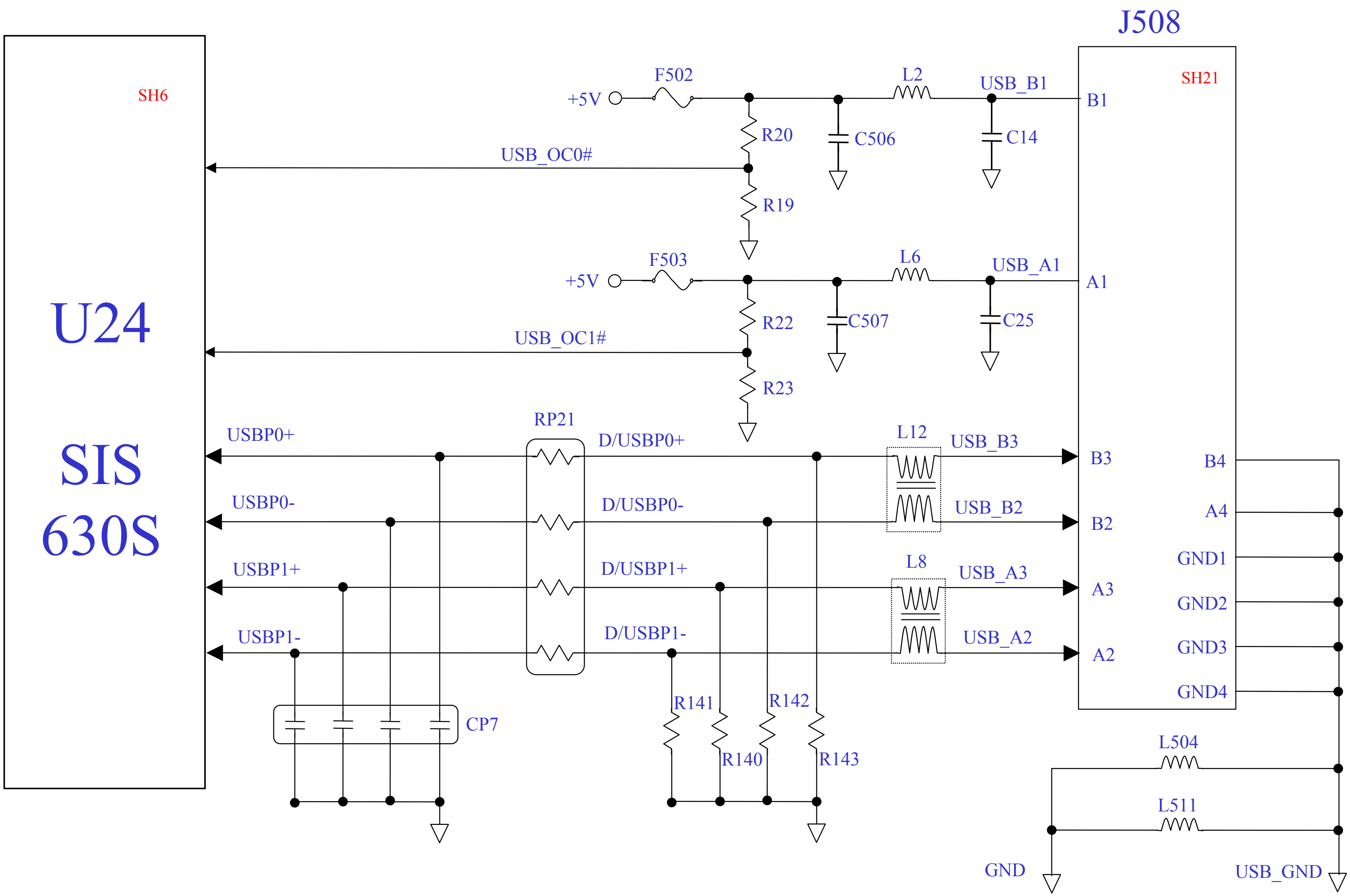
8.8 HARD DRIVE TEST ERROR

Either an error message is shown , or the driver motor continues spinning , while reading data is from or writing data is to hard drive.



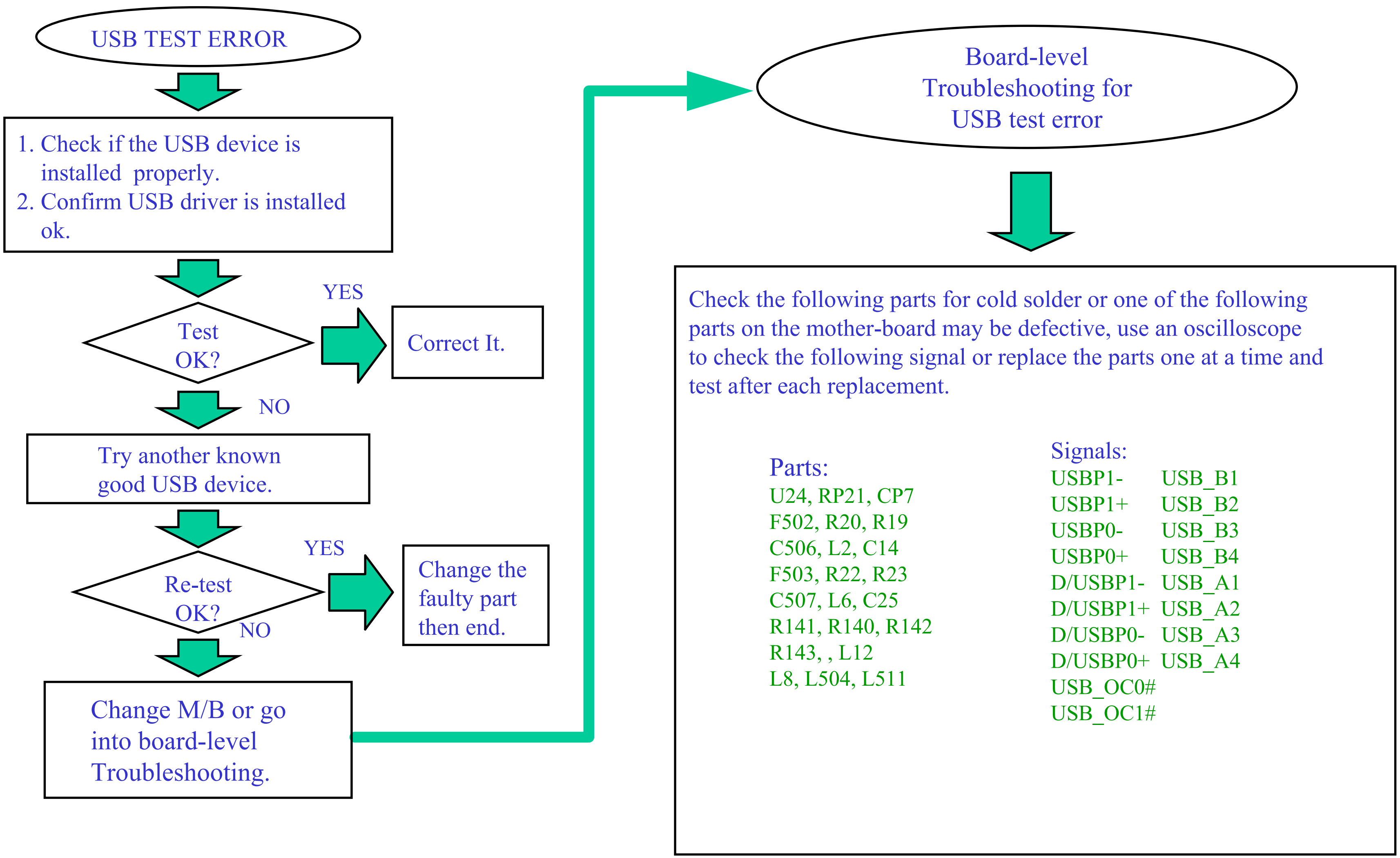
8.9 USB PORT TEST ERROR

An error occurs when a USB I/O device is installed.



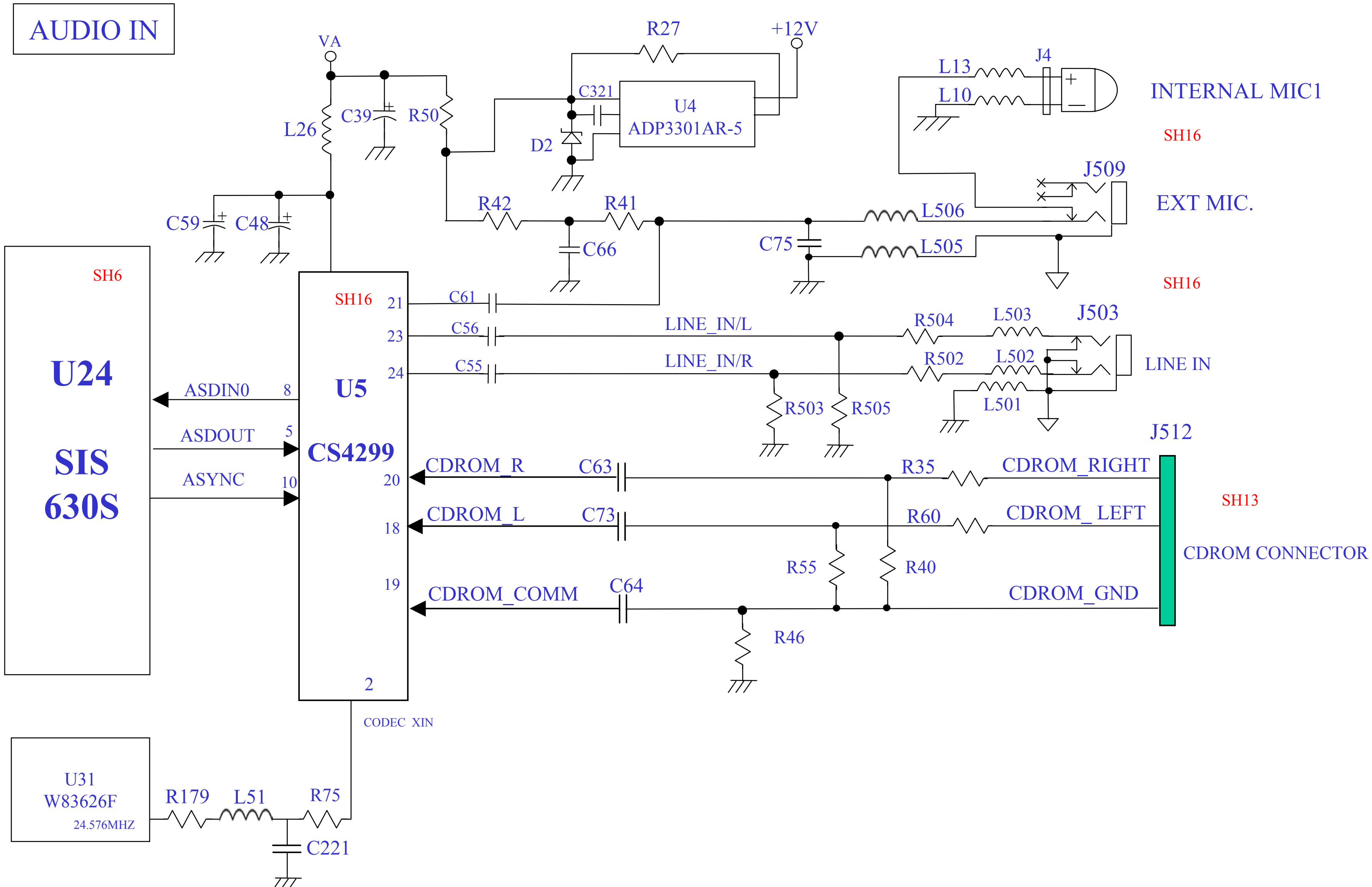
8.9 USB PORT TEST ERROR

An error occurs when a USB I/O device is installed.



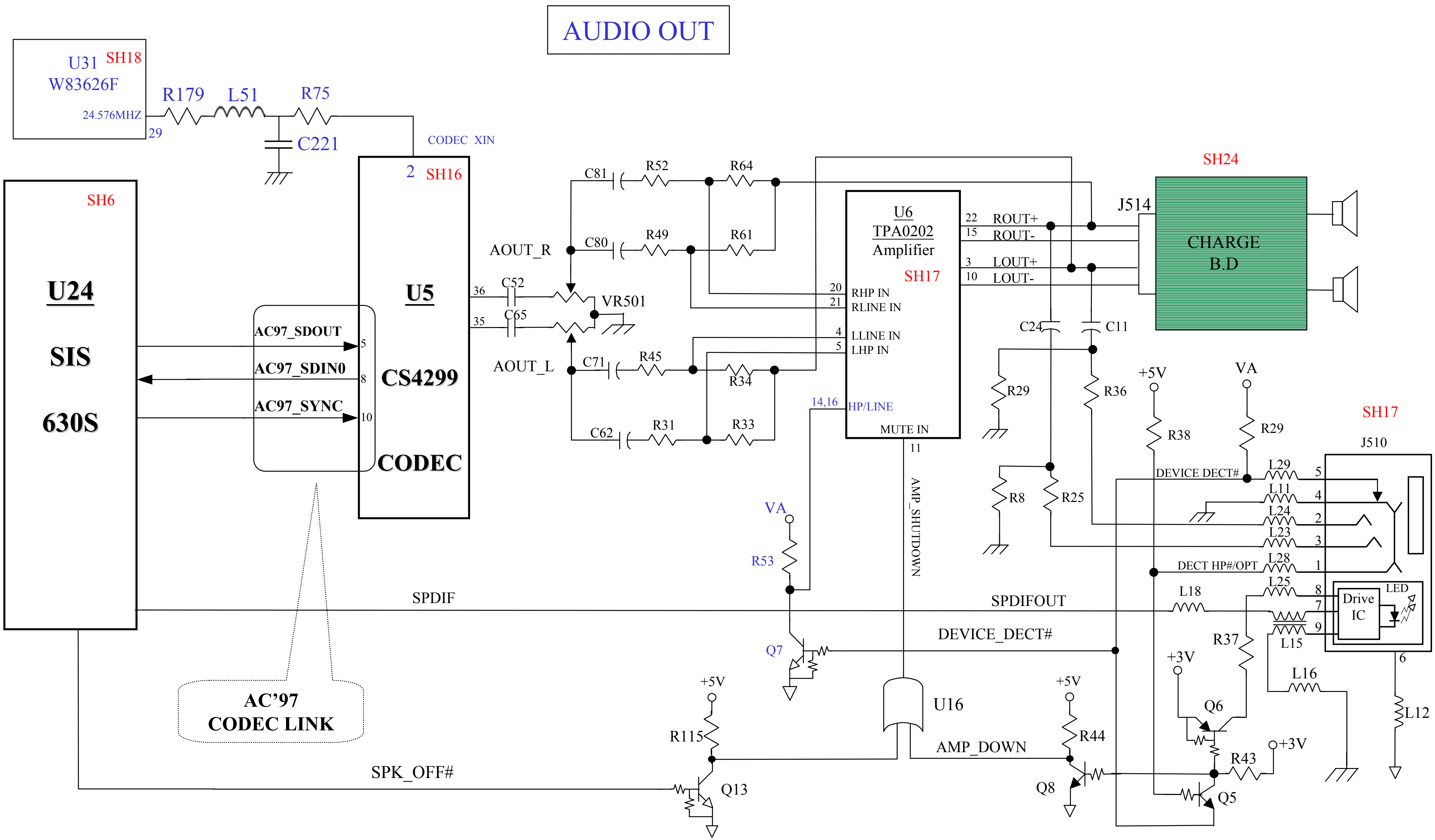
8.10 AUDIO FAILURE

No sound from speaker after audio driver is installed.



8.10 AUDIO FAILURE

No sound from speaker after audio driver is installed.



8.10 AUDIO FAILURE

No sound from speaker after audio driver is installed.

AUDIO DRIVE FAILURE

1. Check if speaker cables are connected properly.
2. Make sure all the drivers are installed properly.

Test OK? — YES: End. — NO:

1. Try another known good speaker, CD-ROM.
2. Exchange another known good charger board.

Test OK? — YES: End. — NO:

Replace M/B or go into board-level Troubleshooting.

Board-level Troubleshooting for audio test error.

Check the following parts for cold solder or one of the following parts on the motherboard may be defective,use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

1. If no sound cause of **line out,** check the following parts & signals:

Parts:	Signals:
U5, C52	AOUT_R
U6, C65	AOUT_L
VR501	ROUT+
C81, C80	ROUT-
C71, C62	LOUT+
R52, R49	LOUT-
R45, R31	SPK_OFF
R64, R61	
R34, R33	
Charge BD	

2. If no sound cause of **MIC**, check the following parts & signals:

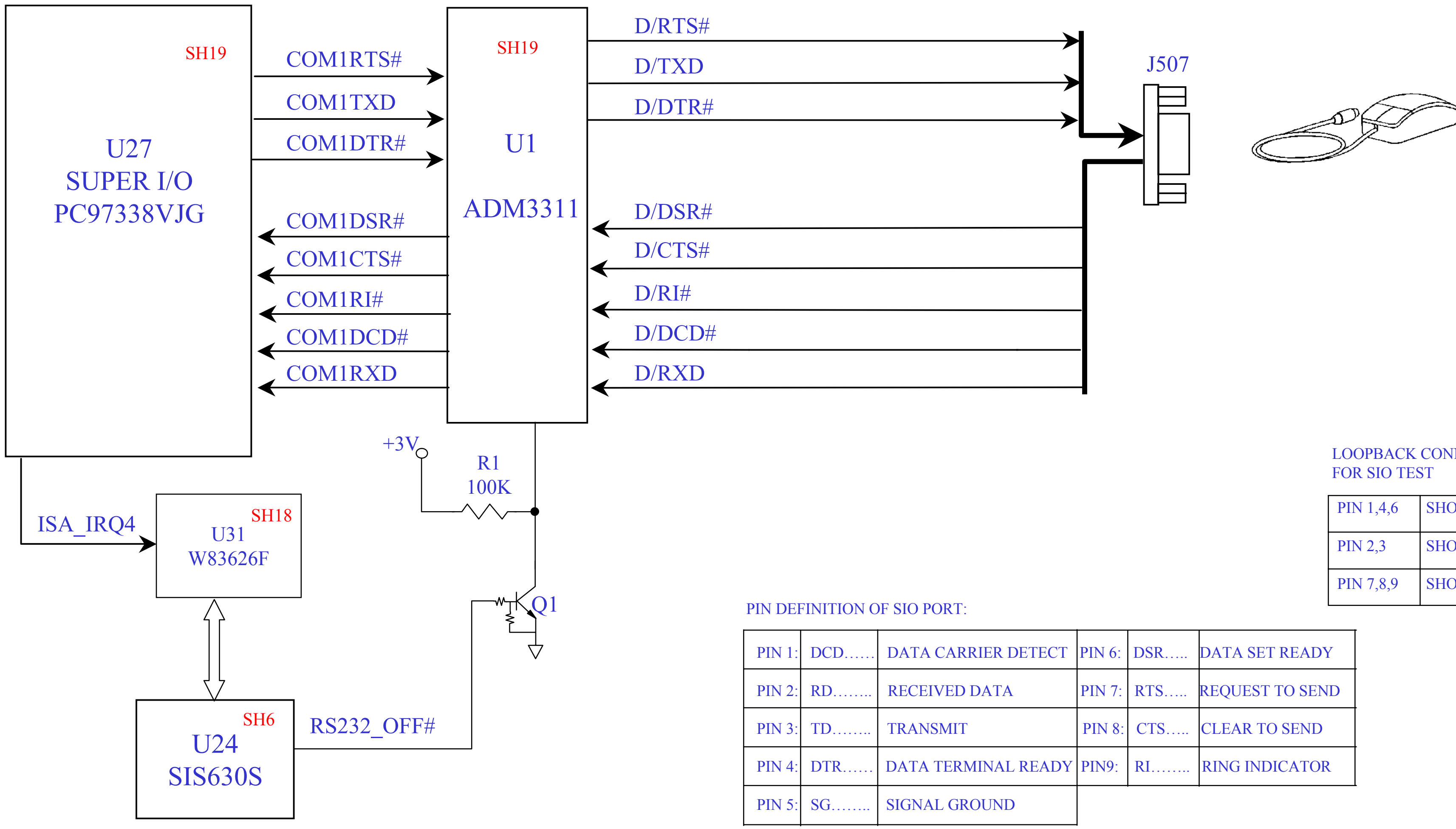
Parts:	Signals:
U5, C61	MIC1
L506, L505	
C75, J509	
J4, L13, L10	
R41, R42	
C39, R50	
D2, U4	

3. If no sound cause of **CD-ROM**,check the following parts & signals:

Parts:	Signals:
U5, C63	CDROM_LEFT
C73, C64	CDROM_RIGHT
J512	CDROM_GND

8.11 SIO PORT TEST ERROR

An error occurs when a mouse or other I/O device is installed.



LOOPBACK CONNECTOR FOR SIO TEST

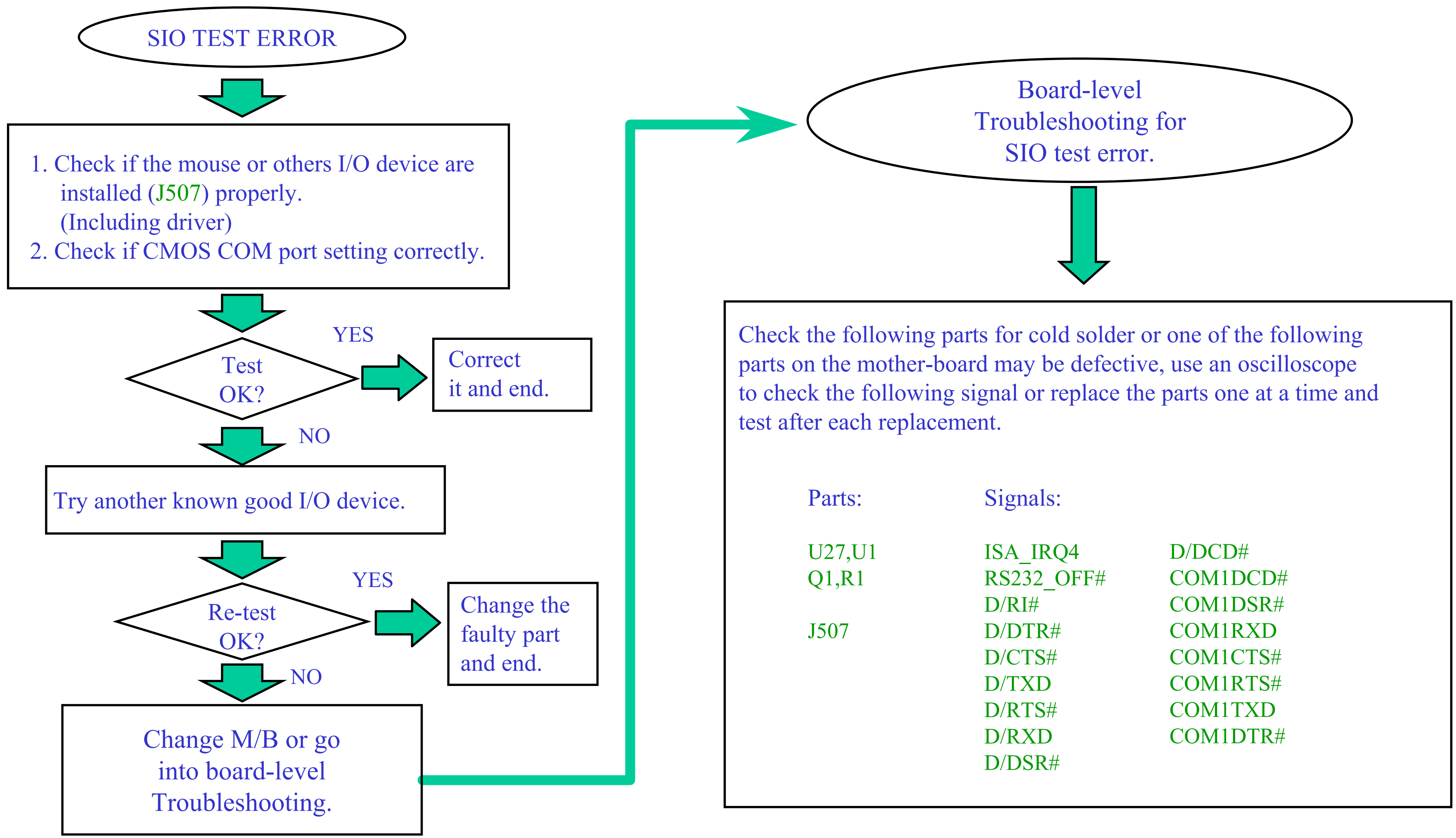
PIN 1,4,6	SHORT
PIN 2,3	SHORT
PIN 7,8,9	SHORT

PIN DEFINITION OF SIO PORT:

PIN 1:	DCD……	DATA CARRIER DETECT	PIN 6:	DSR…..	DATA SET READY
PIN 2:	RD……..	RECEIVED DATA	PIN 7:	RTS…..	REQUEST TO SEND
PIN 3:	TD……..	TRANSMIT	PIN 8:	CTS…..	CLEAR TO SEND
PIN 4:	DTR……	DATA TERMINAL READY	PIN9:	RI……..	RING INDICATOR
PIN 5:	SG……..	SIGNAL GROUND			

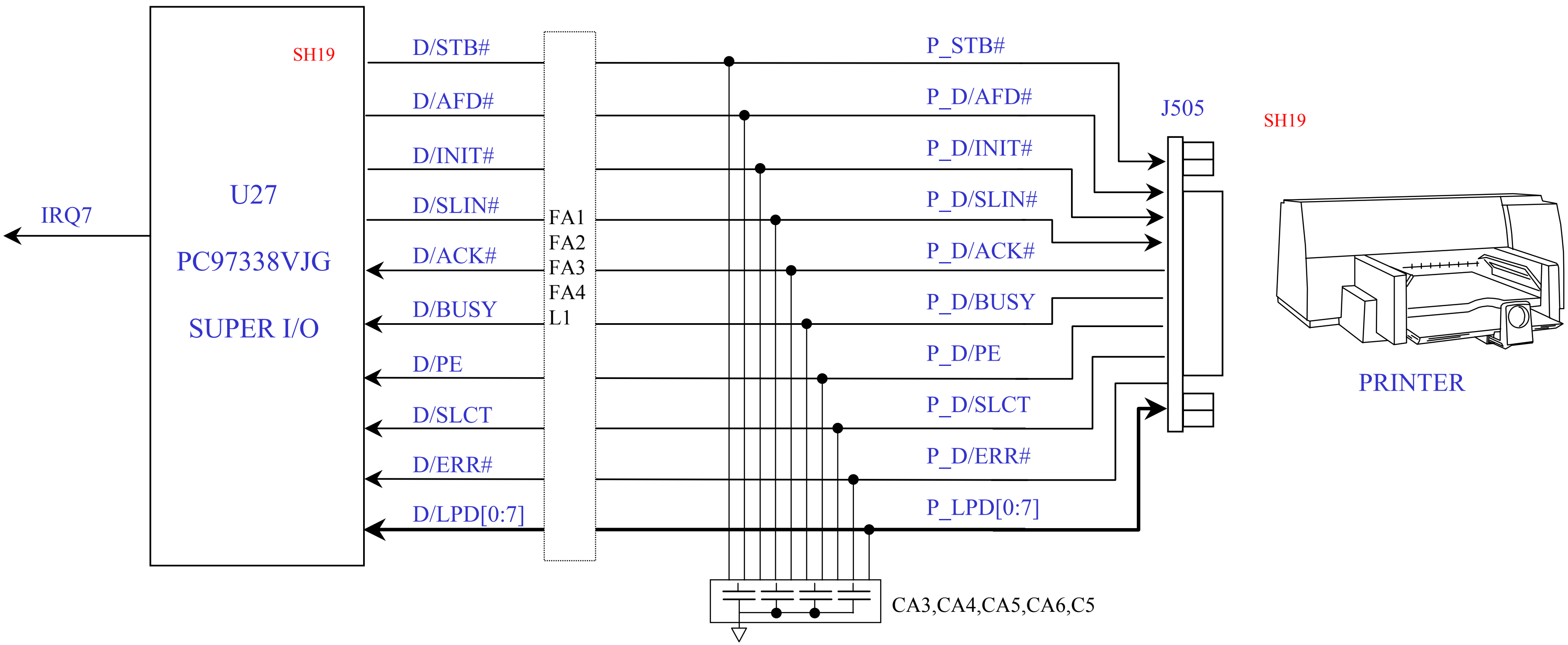
8.11 SIO PORT TEST ERROR

An error occurs when a mouse or other I/O device is installed.



8.12 PIO PORT TEST ERROR

When a print command is issued, printer prints nothing or garbage.



PIN DEFINITION OF PIO PORT

PIN 1	STB	STROBE SIGNAL	PIN 14	AFD	AUTO LINE FEED
PIN 2-9	D0 - D7	PARALLEL PORT DATA BUS D0 TO D7	PIN 15	ERR	ERROR AT PRINTER
PIN 10	ACK	ACKNOWLEDGE HANDSHANK	PIN 16	INIT	INITIATE OUTPUT
PIN 11	BUSY	BUSY SIGNAL	PIN 17	SLIN	PRINTER SELECT
PIN 12	PE	PAPER END	PIN 18-25:	SIGNAL GROUND	
PIN 13	SLCT	PRINTER SELECTED			

LOOPBACK CONNECTOR FOR PIO TEST:

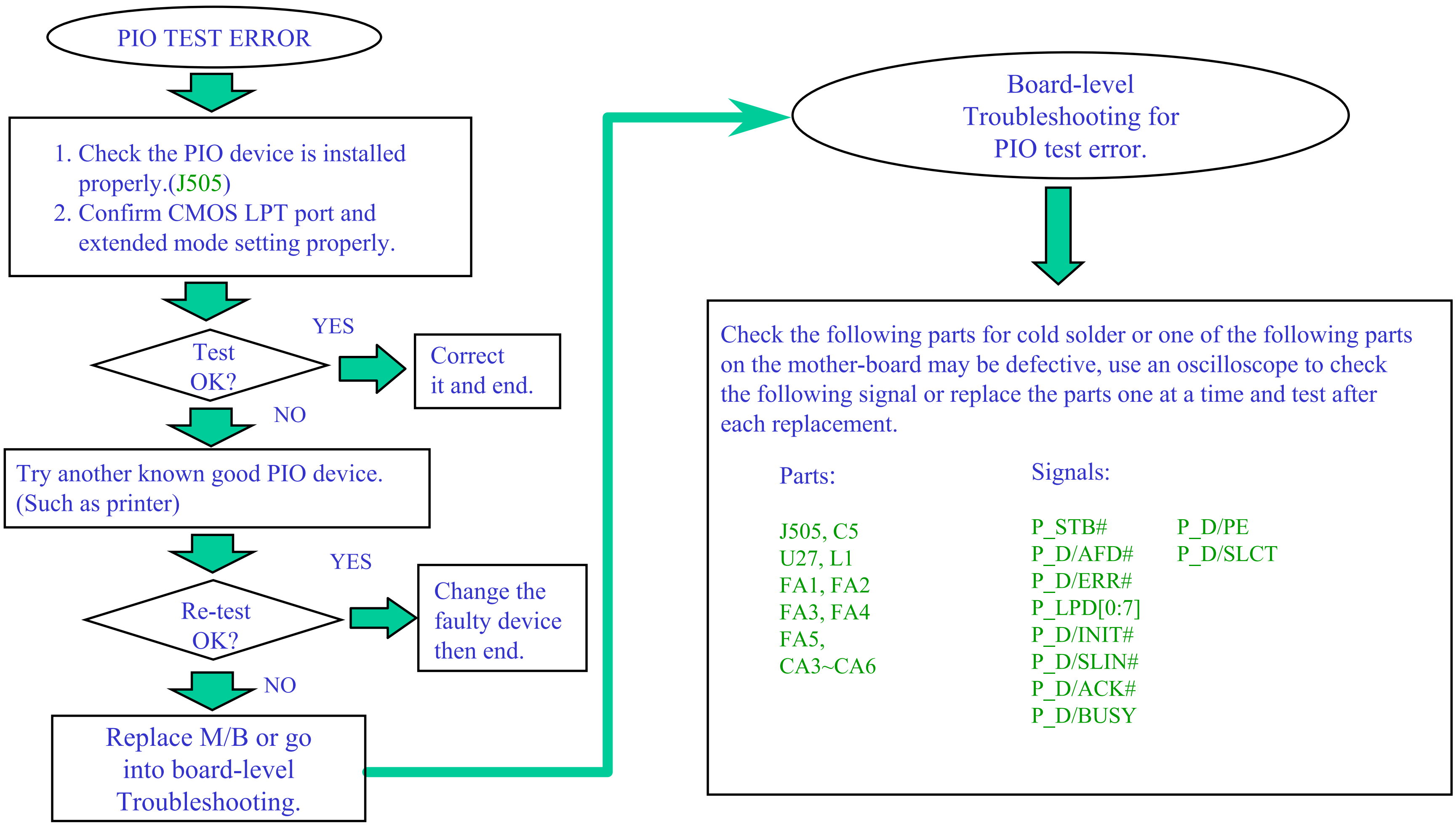
PIN 1, 13	SHORT	PIN 10,16	SHORT
PIN 2, 15	SHORT	PIN 11,17	SHORT
PIN 12, 14	SHORT		

LOOPBACK CONNECTOR FOR EPP TEST:

PIN 1, 2, 4, 6, 8	SHORT
PIN 3, 5, 7, 9, 16	SHORT
PIN 18, 19, 20, 21, 22, 23, 24, 25	SHORT

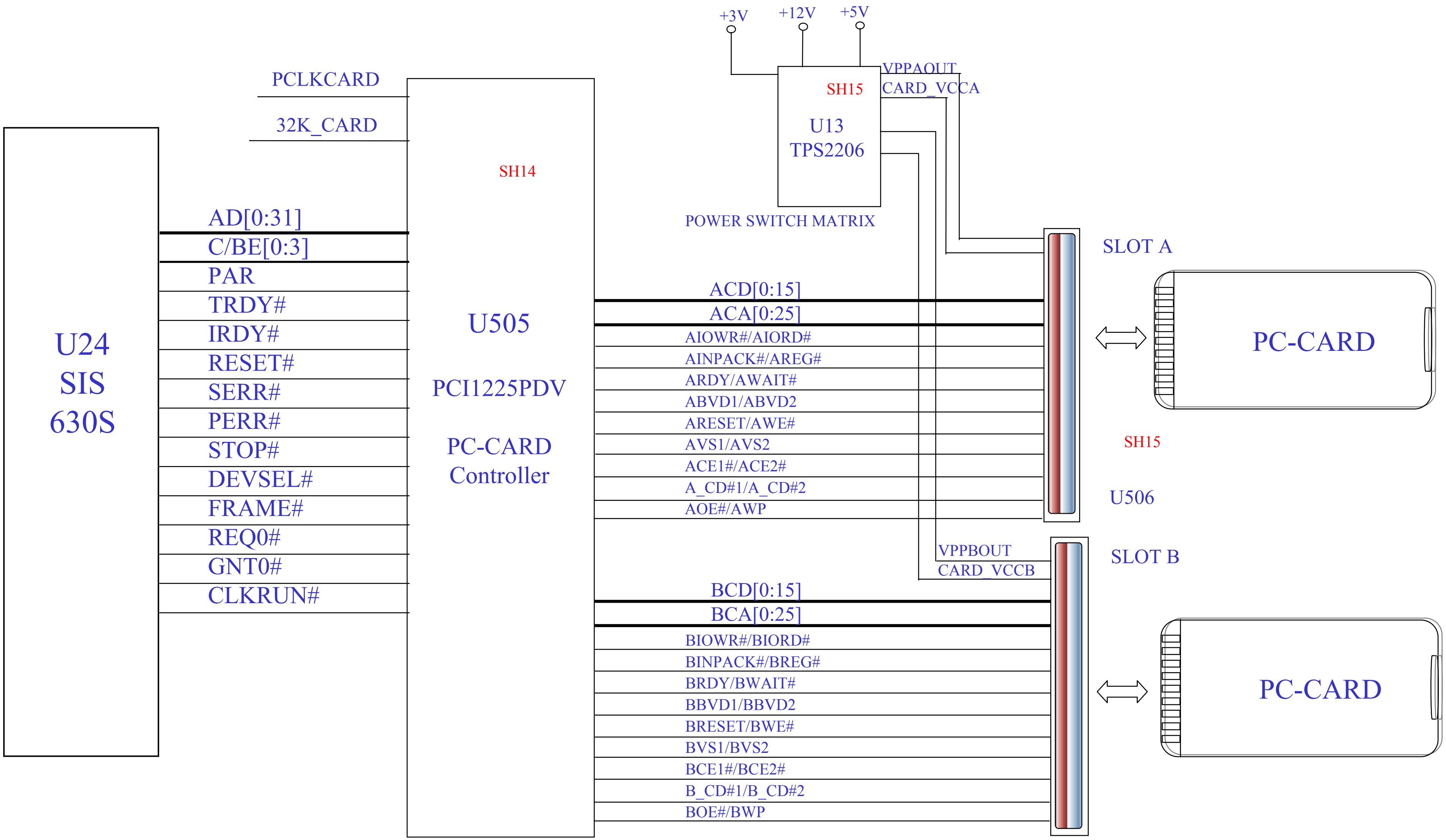
8.12 PIO PORT TEST ERROR

When a print command is issued, printer prints nothing or garbage.



8.13 PC-CARD SOCKET FAILURE

An error occurs when a PC card device is installed.



8.13 PC-CARD SOCKET FAILURE

An error occurs when a PC card device is installed.

PC CARD TEST ERROR

1. Check if the PC CARD device is installed properly.
2. Confirm Pc card driver is installed ok.

Test OK? — YES → Correct It.

NO ↓

Try another known Good PC card device.

Re-test OK? — YES → Change the faulty part then end.

NO ↓

Change M/B or go into board-level Troubleshooting.

→ Board-level Troubleshooting for PC CARD test error

Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:

U13, U505
U506, RP11
RP12, RP14
RP508, RP511
C279, C280
R566, R564
C275, C274
L43, L40, L38
C159, C122
C123, C138
C147, C139
C152, C146

SOCKET A SIGNALS	COMMON SIGNALS	SOCKET B SIGNALS
ACD[0:15]	AD[0:31]	BCD[0:15]
ACA[0:25]	C/BE[0:3]	BCA[0:25]
AIOWR#/AIORD#	PAR	BIOWR#/BIORD#
AINPACK#/AREG#	TRDY#	BINPACK#/BREG#
ARDY/AWAIT#	IRDY#	BRDY/BWAIT#
ABVD1/ABVD2	RESET#	BBVD1/BBVD2
ARESET/AWE#	SERR#	BRESET/BWE#
AVS1/AVS2	PERR#	BVS1/BVS2
ACE1#/ACE2#	STOP#	BCE1#/BCE2#
A_CD#1/A_CD#2	DEVSEL#	B_CD#1/B_CD#2
AOE#/AWP	FRAME#	BOE#/BWP
	REQ0#	
	GNT0#	
	CLKRUN#	

9. SPARE PARTS LIST-1

Part Number	Description	Location(s)
442051200001	AC ADPT ASSY;19V/3.16A,DELTA	
541667000031	AK;1-EN,BOX,7521 MTC CTO	
541667000001	AK;EN,7521-UTILITY ONLY	
441999900047	BATT ASSY OPTION;LI-ION,7521 ID2C	
442670040002	BATT ASSY;14.8V,3.6AH,LI,PAN,ID2 C,7521	
298000000002	BATTERY HOLDER;FOR CR2032,BH-800.1K	BT501
338530010005	BATTERY;LI,3V/220MAH,CR2032	
340670020005	BEZEL ASSY;DVD-ROM,PIONEER,7521P	
221670040001	BOX;AK,7521	
340669600048	BRACKET ASSY-4;I/O,TV-OUT,RACE	
342670000003	BRACKET; LCD,UNIPAC,L,7521	
342670000004	BRACKET; LCD,UNIPAC,R,7521	
342669600014	BRACKET;CD-ROM,RACE	
342666600002	BRACKET;HDD,TITAN	
344670000005	BUTTON;TOUCH PAD,7521	
421015560001	CABLE ASSY;PHONE LINE,6P2C,W/Z CORE	
421015560001	CABLE ASSY;PHONE LINE,6P2C,W/Z CORE	
332300000115	CABLE;FFC,FDD,6020	
332669600002	CABLE;FFC,IQSB BD,CHARGER BD,REDSEA	
332669600001	CABLE;FFC,TOUCHPAD,REDSEA	
272075103501	CAP;.01U ,50V ,20%,0603,X7R,SMT	PC104,PC98,C290,PC102
272075103702	CAP;.01U ,50V,+80-20%,0603,SMT	C27,C32,C34,C590,C600,
272075103401	CAP;.01U ,CR,50V ,10%,0603,X7R,SMT	PC118,PC121,PC124,PC1
272005103401	CAP;.01U ,CR,50V,10%,0805,X7R	C174
272072104702	CAP;.1U ,16V,+80-20%,0603,SMT	C1,C103,C122,C123,C129

Part Number	Description	Location(s)
272073104501	CAP;.1U ,25V,+80-20%,0603,Y5V,SMT	C525,C540,C549,C559,C5
272075104701	CAP;.1U ,50V,+80-20%,0603,SMT	C143,C149,C160,C165,C1
272072104402	CAP;.1U ,CR,16V,10%,0603,X7R,SMT	C10,C501,C517,C527,C53
272002474401	CAP;.47U ,CR,16V ,10%,0805,X7R,SMT	C12
272030102401	CAP;1000P,2KV,10%,1808,X7R,SMT	C17
272075102701	CAP;1000P,50V ,+/-20%,0603,X7R,SMT	C126,C134,C14,C25,C27
272075102403	CAP;1000P,CR,50V,10%,0603,X7R,SMT	PC51,PC58,PC60,PC63,P
272075101701	CAP;100P ,50V ,+ -10%,0603,NPO,SMT	C100,C101,C133,C5,C50
272075101401	CAP;100P ,50V ,10%,0603,COG,SMT	C505
272075100701	CAP;10P ,50V ,+-10%,0603,NPO,SMT	C113,C114,C116,C117,C1
272075100401	CAP;10P ,50V ,10%,0603,COG,SMT	C106,C514,C671
272021106501	CAP;10U ,10V ,20%,1210,X7R,SMT	C506,C507,PC7,PC83,PC
272011106701	CAP;10U ,10V,+80-20%,1206,Y5V,SMT	C223,C243,C244,C624,C6
272012106701	CAP;10U ,16V ,+80-20%,1206,Y5U,SMT	C109,C112,C121,C179,C1
272022106701	CAP;10U ,16V,+80-20%,1210,Y5V,SMT	C226,C39
272023106501	CAP;10U ,25V ,20%,1210,Y5U,SMT	PC14,PC35,C255,PC108,
272431157504	CAP;150U ,4V ,20%,7343,POSCAP,SMT	PC70,C124,PC119,PC120
272431157505	CAP;150U ,6.3V ,20%7343,POSCAP,SMT	PC10
272001105403	CAP;1U ,10%,10V ,0805,X7R,SMT	C518,C519,C520,C526,C5
272071105701	CAP;1U ,CR,10V ,80-20%,0603,Y5V	C195,C46,C537,C54,C57
272012105702	CAP;1U ,CR,16V ,+80-20%,1206,Y5V	C250,C263,C679
272013105501	CAP;1U ,CR,25V ,+80-20%,1206,SMT	PC18
272002105701	CAP;1U ,CR,16V ,-20+80%,0805,Y5V,S	C139,C146,PC510,PC97,
272002225701	CAP;2.2U ,CR,16V ,+80-20%,0805,Y5V	C55,C56
272012225702	CAP;2.2U ,CR,16V ,+80-20%,1206,Y5V	C147,C152,C37

9. SPARE PARTS LIST-2

Part Number	Description	Location(s)
272075222701	CAP;2200P,50V ,+/-20%,0603,X7R,SMT	C107
272075221302	CAP;220P ,50V ,5% ,0603,NPO,SMT	C23,C31,PC76,PC77
272075220701	CAP;22P ,50V ,+ -10%,0603,NPO,SMT	C108,C128
272021226701	CAP;22U ,10V,+80-20%,1210,Y5V,SMT	C154,PC519
272041226501	CAP;22U ,CR,10V ,20%,1812,X7R,SMT	C547
272011475401	CAP;4.7U ,10%,10V ,1206,X7R,SMT	C175
272001475701	CAP;4.7U ,CR,10V ,+80-20%,0805,Y5V,	C184,C20,C227,C36,C12
272012475701	CAP;4.7U ,CR,16V ,+80-20%,1206,Y5V	C521,C522,C523,C528,C5
272075471401	CAP;470P ,50V,10%,0603,X7R,SMT	PC116
272075470401	CAP;47P ,50V ,10%,0603,COG,SMT	C150,C157,C158,C163,C1
221670020009	CARTON;NON-BRAND,TW,7521	
431670020003	CASE KIT;ID3C 7521P MTC	
342665500008	CFM-SUYIN;S-STANDOFF,#4-40H4.8,NIW	
273000111002	CHOKE COIL;120OHM/100MHZ,20%,3216	L12,L15,L544,L545,L8
313000020248	CHOKE COIL;15UH,16.5TS,55130,TUBE	PL502
273000500023	CHOKE COIL;1UH ,20%,15A,3.5MM,SMT	PL11
273000500034	CHOKE;10UH,3.5A,3.65mm,THA02P63,SMT	PL6,PL8
313000020148	CHOKE;15UH,D.7*16T/.2*32,55130,TUBE	PL503
331720015023	CON;D,FM,15P,2.29,R/A,3 ROW,TITAN	J506
331720025012	CON;D,FM,25P,2.77,R/A,TITAN	J505
331720009008	CON;D,MA,9P,2.775,R/A,TITAN	J507
291000151204	CON;FPC/FFC,12P,.5MM,R/A,SMT,REDSEA	J515
291000152604	CON;FPC/FFC,26P,1MM,R/A,ELCO,SMT	J5
291000023002	CON;HDR,FM,15P*2,0.8MM.H4.4,R/A,SMT	J511
291000023201	CON;HDR,FM,16P*2,1.27MM,R/A,SMT	J514

Part Number	Description	Location(s)
291000010604	CON;HDR,FM,6P*1,1.25MM,ST,SMT	J1
291000012011	CON;HDR,MA,10P*2,1.0MM,ST,SMT	J2
331040060003	CON;HDR,MA,20P*3,.8MM,R/A,AMP	J516
291000025006	CON;HDR,MA,25P*2,.8MM,R/A,SMT	J512
291000011410	CON;HDR,MA,7P*2,1.27MM,ST,H3MM,SMT	J3
291000251441	CON;IC CARD,FM,72P*2,.6MM,H3MM,SMT	U506
331870004005	CON;MINI DIN,4P,R/A,W/GROUNDING,F6S	J501
331870006013	CON;MINI DIN,6P,R/A,W/GROUND,73156	J502
291000810805	CON;PHONE JACK,8P,H=12.59,R/A,RJ45,C100	J504
331910003020	CON;POWER JACK,3P,D=2.5,MARLIN	PJ501
331840010001	CON;STEREO JACK,10P,W/SPDIF,R/A	J510
331840005007	CON;STEREO JACK,5P,R/A,W9.1,LGY2313	J503,509
331000008026	CON;USB,FM,H=13.62,R/A,4P*2,72309-6220B	J508
291000410201	CON;WFR,MA,2P,1.25,ST,SMT/MB	J4
291000410301	CON;WFR,MA,3P,1.25,ST,SMT/MB	J513
345669600065	CONDUCTIVE TAPE;MB,SDRAM,RACE	
345669600053	CONDUCTIVE TAPE;PCMCIA,RACE	
313000150093	CORE;LAN CORE,230OHM/100MHZ,LF-100	
340670020009	COVER ASSY;CPU,7521P	
340670000031	COVER ASSY;EASY STAR,ID3,CHAMP,7521	
340670000015	COVER ASSY;LCD,ID2,CHAMP,7521	
441670020003	COVER ASSY;M/B,14",ID3C 7521P MTC	
344670000051	COVER HINGE;ID2,CHAMP,7521	
344670000013	COVER;MODEM,7521	
272625101401	CP;100P*4,8P,50V ,10%,1206,NPO,SMT	CA3,CA4,CA5,CA6

9. SPARE PARTS LIST-3

Part Number	Description	Location(s)
272625470401	CP;47P*4 ,8P,50V ,10%,1206,NPO,SMT	CA501,CA502,CA7,CA8,C
345669600062	CUSHION;CPU-1,RACE	
291006214411	DIMM SOCKET;144P,.8MM,AMP353870,SMT	J6
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	PD10,PD11,PD14,PD15,I
288100701002	DIODE;BAV70LT1,70V,225MW,SOT-23	D502
288100099001	DIODE;BAV99,70V,450MA,SOT-23	D5,D6,D7,D9
288100056003	DIODE;BAW56,70V,215MA,SOT-23	D17
288100212001	DIODE;DAN212K,80V,SWITCH,SOT23	D18
288101004024	DIODE;EC10QS04,RECT,40V,1A,CHIP,SMT	PD7,PD8,PD1,PD2,PD20
288103104001	DIODE;EC31QS04-TE12L,40V,3A,SMT	PD18,PD19,PD3,PD4,PD
288104148001	DIODE;RLS4148,200MA,500MW,MELF,SMT	D1,D14,D16,D19,D501,D
288100020001	DIODE;RLZ20C,ZENER,19.23V,5%,SMT	PD506
288100024002	DIODE;RLZ24D,ZENER,23.63V,5%,SMT	PD501
288100056001	DIODE;RLZ5.6B,ZENER,5.6V,5%,LL34	D505,D15,D20
288100056005	DIODE;UDZ5.6B,ZENER,5.6V,UMD2,SMT	D2,D506
451670000102	DVD ME KIT;8X,DVD-K11,7521	
523467000005	DVD ROM ASSY;8X,K11TA,7521	
272601107506	EC;100U ,6.3V,M,9.3*3.6,-55~105'C	C11,C24
312271006358	EC;100U,25V,RA,M,D6.3*7,SGX,SANYO	PC503,PC508
312272205359	EC;22U ,20V,20%,RA,D6.3*5,OS-CON	PC521
272603226505	EC;22U ,20V,M,SVP,6.6mm,OS-CON,SMT	PC127
272601337502	EC;330u ,6.3V,M,10.1*4.6,-55~105'C	C4
312270687161	EC;680U,6.3V,20%D10,FUJITSU-FPCAP	PC512,PC513
227670000003	END CAP;AK BOX,7521	
227670000004	END CAP;BATTERY,7521	

Part Number	Description	Location(s)
227670000002	END CAP;MANUAL,7521	
227670000010	END CAP;W/CARRING BAG,7521	
481670000002	F/W ASSY;KBD CTRL,7521+	U14
481670000001	F/W ASSY;SYS/VGA BIOS,7521+	U28
523411442008	FD DRIVE;1.44M,3 MODE,D353G	
523467002001	FDD ASSY;7521P ID3C MTC	
273000610013	FERRITE ARRAY;120OHM100MHZ,3216,MAG	FA1,FA10,FA11,FA2,FA3,
273000610014	FERRITE ARRAY;60OHM/100MHZ,3216,MAG	RP58
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,6A	L532,L533,L56,PL1,PL50
273000150031	FERRITE CHIP;120OHM/100MHZ,2012,SMT	L9,L2,L3,L4,L55,L6
273000130039	FERRITE CHIP;130OHM/100MHZ,1608,SMT	L33,L36,L37,L38,L39,L40
273000150036	FERRITE CHIP;32OHM/100MHZ,2012,SMT	C102,C16,L21,R10,R73
273000130006	FERRITE CHIP;600OHM/100MHZ,.2A,1608	L504,L511
273000130038	FERRITE CHIP;600OHM/100MHZ,1608,SMT	L10,L11,L13,L16,L18,L23
273000150022	FERRITE CHIP;60OHM/100MHZ,2012,SMT	L20,L5
346664900010	FILM;LCD PROTEC,.14.2",235*300,5027	
288003600001	FIR;HSDL3600#007,FRONT VIEW,10P,SMT	U501
295000010008	FUSE;1.1A,POLY SWITCH,1812,SMT	F1
295000010014	FUSE;1.1A/6V,POLY SWITCH,PTC,SMD	F502,F503
295000010105	FUSE;1A,NORMAL,1206,SMT	F2
295000010029	FUSE;FAST,.75A,63V,1206,THIN FILM	PF1
295000010016	FUSE;NORMAL,6.5A/32VDC,3216,SMT	PF501
345669600055	GASCKET;TV-OUT,RACE	
345669600047	GASKET;FDD,LONG,RACE	
345669600048	GASKET;FDD,SHORT,RACE	

9. SPARE PARTS LIST-4

Part Number	Description	Location(s)
345669600006	GASKET;IO-PS2,RACE	
345669600013	GASKET;LAN,RACE	
345669600041	GASKET;LVDS,9X6X10,RACE	
345669600043	GASKET;MIC,5X5X19,RACE	
345669600042	GASKET;USB,10X15X0.3,RACE	
345669600005	GASKET;USB,RACE	
523415780091	HD DRIVE;20GB,2.5",MHM2200AT,9.5,F	
451670040004	HDD ME KIT;7521 ID2 C	
523499990051	HDD OPTION;20GB,9.5MM	
340670020007	HEATSINK ASSY;CPU,7521P	
451670000131	HEATSINK ME KIT;7521	
340670020012	HOUSING ASSY;LCD,CHIMEI,ID3C,7521P	
340670020002	HOUSING ASSY;TV-OUT;7521P	
451670020031	HOUSING KIT+TV-OUT;14",7521P ID3C	
344670000054	HOUSING;FDD-HDD,ID2,CHAMP,7521	
344600000239	IC CARD CON PART;72P*2,22RRF	
331650037002	IC SOCKET;370P,ZIF,ZIFPGA370	U503
282574132001	IC;74AHCT1G32,SINGLE OR GAT,SOT23-5	U8
282574032006	IC;74AHCT32,QUAD 2-I/P OR,TSSOP,14P	U16
282074338405	IC;74CBT3384,10 BIT BUS SW,TSOP-24	U507
282074244005	IC;74LVC244A,BUFFER,TSSOP,20P	U508
282574164002	IC;74VHC164,SIPO REGISTER,TSSOP,14P	U3
284501021003	IC;ADM1021A,TEMPERATURE MTR,SSOP16	U9
286203311001	IC;ADM3311E,RS-232,TSSOP,28P	U1
286300809003	IC;ADM809M,RESET CIRCUIT,4.38V,SOT2	U504

Part Number	Description	Location(s)
286303301001	IC;ADP3301AR-5,.8%,REG.,SO,8P	U4
284507005001	IC;CH7005C,TV ENCODER,3/5V,PQFP,44P	U7
324180786043	IC;CPU,P-III,800MHZ,EB,FCPGA,370P	
284504299001	IC;CS4299-JQ,AC97 CODEC,TQFP,48P	U5
284590363001	IC;DS90C363,LVDS,18BIT,SSOP,48P	U2
283466570001	IC;EEPROM,9346,64*16 BITS,SO8,SMT	U17
283450083001	IC;FLASH,256K*8-70,PLCC32,ST39SF020	
284583434001	IC;H8/F3434,KBD CTLR,TQFP,100P	
286317812001	IC;HA178L12UA,VOLT REGULATOR,SC-62	PU501
284509248006	IC;ICS9248-102,CLOCK GEN,SSOP,48P	U15
286100393002	IC;LM393A,DUAL,COMPARTOR,SO,8P	U33
286100393004	IC;LMV393,DUAL COMPARTOR,SSOP,8P	PU3
286302951015	IC;LP2951ACM,VOLTAGE REGULATOR,SO	U20,U32
286301628001	IC;LTC1628,PWM SWITCH REG.,SSOP,28P	PU14
286301632002	IC;MAX1632CAI,PWM CTRL,SSOP,28P	PU10
286301711001	IC;MAX1711/PWM CTLR,SOP,24P	PU18
286300809002	IC;MAX809S,RESET CIRCUIT,2.9V,SOT23	U10,U12
284597338001	IC;PC97338VJG,SUPER I/O,TQFP,100P	U27
284501225001	IC;PCI1225PDV,PCI/CARDBUS,LQFP,208P	U505
286300431010	IC;SC431CSK-1,1%,ADJ REG,SOT23	Q28
286300431014	IC;SC431LCSK-.5,.5%,ADJ REG,SOT23	PQ11,PQ14,PQ8
283767002002	IC;SDRAM,2M*16*4-133,TSOP,54P,7521P,SIS	U18,U19,U22,U23,U25,U
284500630009	IC;SIS630S,PCI/AGP/LPC,VGA,BGA,672P	U24
284500900001	IC;SIS900,LAN CONTROLLER,PQFP,128P	U21
286300594001	IC;TL594C,PWM CONTROL,SO,16P	PU17

9. SPARE PARTS LIST-5

Part Number	Description	Location(s)
286100202001	IC;TPA0202,AUDIO AMP,2W,TSSOP,24P	U6
286302216001	IC;TPS2216,CARDBUS PWM CTRL,SSOP30P	U13
284583601001	IC;W83601R,I2C TO GPIO,SSOP 20P	U11
284583626001	IC;W83626F,LPC/ISA BRIDGE,PQFP,128P	U31
273000114002	INDUCTER;4.7UH,10%,1206,SMT	L522
273000990021	INDUCTOR;33uH,CDRH124,SMT	PL506
346669600056	INSULATOR 4X50X0.5;I/O BRACKET,RACE	
346669600055	INSULATOR 4X8X0.5;I/O BRACKET,RACE	
346669600054	INSULATOR;DC JACK,RACE	
346669600071	INSULATOR;FDD BACK,RACE	
346669600014	INSULATOR;INVERTER,REDSEA	
346669600041	INSULATOR;MEMORY,RACE	
346670020001	INSULATOR;PCMCIA,7521P	
346669600039	INSULATOR;TP BUTTON,RACE	
346670020005	INSULATOR;TV-OUT,7521P	
531020237254	KBD;87,UI,K982318S1,W/EMI,7521	
451670000058	LABEL KIT;NON-BRAND,7521 MTC	
242600000380	LABEL;10*8MM,BIOS,HI-TEMP 260	
242600000380	LABEL;10*8MM,BIOS,HI-TEMP 260	
242662300009	LABEL;25*10MM,3020F	
242600000385	LABEL;27*10,LAN ID BAR CODE	
242600000378	LABEL;27*7MM,HI-TEMP 260'C	
242670020001	LABEL;AGENCY-GLOBAL,MTC,7521	
242600000157	LABEL;BAR CODE & S/N,13.5*75,COMMON	
242600000433	LABEL;BLANK,11*5MM,COMMON	

Part Number	Description	Location(s)
242664800013	LABEL;CAUTION,INVERT BD,PITCHING	
242600000099	LABEL;MODEL,5M,MITAC	
242600000001	LABEL;PAL,20*5MM,COMMON	
242600000412	LABEL;PENTIUM,PWR SUITE 3 NOTE BIOS	
242668800033	LABEL;WINDOWS ME,CARTON,ORION2	
242668820022	LABEL;WINDOWS ME/2000,ORION-3	
441670020032	LCD ASSY;TFT,CHIMEI,14",7521P ID3C	
451670020002	LCD ME KIT;TFT,CHIMEI,14",7521P ID3C	
413000020266	LCD;N141X201,TFT,14",LVDS,XGA,CHIMEI	
561567000001	MANUAL KIT;EN,7521,NON-BRAND	
561567000031	MANUAL;USER'S,EN,7521,NON-BRAND	
421670000031	MICROPHONE ASSY;LCD,7521,MSL	
412999900007	MODEM OPTION;UNIVERSAL,MDC,7521	
416267002013	NB PLATFORM;TFT,CHIMEI,14",7521P ID3C M	
274042500405	OSC;25MHZ,50PPM,3.3V,15PF,H=1,SMALL	OSC1
461670000015	PACKING KIT;N-B,BOX,7521 MTC	
221670050001	PARTITION;AK BOX,7521	
221670050007	PARTITION;STOPER,AK BOX,7521	
412155600048	PCB ASSY;MDM,56K,UNIV,W/O Y-CAP,7521	
222600020049	PE BAG;50*70MM,W/SEAL,COMMON	
222600020049	PE BAG;50*70MM,W/SEAL,COMMON	
222667220003	PE BAG;L560XW345,CERES	
222670000001	PE BUBBLE BAG;BATTERY,7521	
340669600004	PLATE ASSY;TOUCHPAD,REDSEA	
412670050004	PWA;PWA-7521 ID3C,QSB TRANS BD,MTC	

9. SPARE PARTS LIST-6

Part Number	Description	Location(s)
412670000005	PWA;PWA-7521,CHARGER TRANS BD MTC	
412670000001	PWA;PWA-7521,HDD/FDD BD,T/U MTC	
412670000004	PWA;PWA-7521,IQSB TRANS BD,T/U MTC	
412670000002	PWA;PWA-7521,MDC TRANS BD,MTC	
411670020002	PWA;PWA-7521P,MOTHER BD MTC	
411670020004	PWA;PWA-7521P,MOTHER BD,SMT MTC	
411670020003	PWA;PWA-7521P,MOTHER BD,T/U MTC	
412670000006	PWA;PWA-INVERTER BD,7521,T/U,MTC	
332810000033	PWR CORD;125V/7A,2P,BLACK,AMERICA	
271045157101	RES;.015 ,1W ,1% ,2512,SMT	PR1,PR3,PR32,PR35
271045207101	RES;.02 ,1W ,1% ,2512,SMT	PR68,PR2
271002000301	RES;0 ,1/10W,5% ,0805,SMT	L507
271071000002	RES;0 ,1/16W,0603,SMT	L52,L541,PR12,PR30,R11
271071100302	RES;10 ,1/16W,5% ,0603,SMT	R163,R527,R154,R162
271071101301	RES;100 ,1/16W,5% ,0603,SMT	R599
271071104101	RES;100K ,1/16W,1% ,0603,SMT	PR18
271071104302	RES;100K ,1/16W,5% ,0603,SMT	PR21,PR48,PR5,PR501,P
271071103101	RES;10K ,1/16W,1% ,0603,SMT	PR26,PR27,PR37,PR38,P
271071103302	RES;10K ,1/16W,5% ,0603,SMT	R127,R149,R150,R152,R1
271071106301	RES;10M ,1/16W,5% ,0603,SMT	R120
271071118271	RES;11.8K,1/16W,0.1%,0603,SMT	PR61
271071111101	RES;110 ,1/16W,1% ,0603,SMT	R553,R558
271071124102	RES;12.4K ,1/16W,1% ,0603,SMT	PR47
271071124301	RES;120K ,1/16W,5% ,0603,SMT	PR14
271071141102	RES;140 ,1/16W,1% ,0603,SMT	R581

Part Number	Description	Location(s)
271071143701	RES;14K ,1/16W,0.1% ,0603,SMT	R30
271072151101	RES;150 ,1/10W,1% ,0603,SMT	R519,R542,R547,R555,R5
271071153101	RES;15K ,1/16W,1% ,0603,SMT	PR45
271071153301	RES;15K ,1/16W,5% ,0603,SMT	R140,R141,R142,R143,R3
271071178311	RES;178K ,1/16W,1% ,0603,SMT	R204
271071102302	RES;1K ,1/16W,5% ,0603,SMT	PR22,PR39,R211,R29,R5
271071105101	RES;1M ,1/16W,1% ,0603,SMT	R568,PR83
271071105301	RES;1M ,1/16W,5% ,0603,SMT	PR13,PR64,PR72,PR73,R
271071222302	RES;2.2K ,1/16W,5% ,0603,SMT	R2,R3,R63,R169
271071272301	RES;2.7K ,1/16W,5% ,0603,SMT	R128,R129,R130,R161,R6
271071200101	RES;20 ,1/16W,1% ,0603,SMT	PR75
271071203101	RES;20K ,1/16W,1% ,0603,SMT	R35,R60,R228
271071221302	RES;22 ,1/16W,5% ,0603,SMT	R103,R131,R132,R133,R1
271071221301	RES;220 ,1/16W,5% ,0603,SMT	R507,R557,R67
271071226311	RES;226K ,1/16W,1% ,0603,SMT	PR16
271071249811	RES;24.9 ,1/16W,1% ,0603,SMT	R254,R255,R257,R258
271071249311	RES;249K ,1/16W,1% ,0603,SMT	PR65
271071202102	RES;2K ,1/16W,1% ,0603,SMT	PR66,PR71
271071202301	RES;2K ,1/16W,5% ,0603,SMT	PR44
271071205101	RES;2M ,1/16W,1% ,0603,SMT	R571
271071316211	RES;31.6K,1/16W,1% ,0603,SMT	PR55,PR81
271071330302	RES;33 ,1/16W,5% ,0603,SMT	PR4,PR502,PR506,R112,
271071331301	RES;330 ,1/16W,5% ,0603,SMT	R27,R508,R517,R548,R5
271071333301	RES;33K ,1/16W,5% ,0603,SMT	PR23,PR509,R34,R61
271071357311	RES;357K ,1/16W,1% ,0603,SMT	PR80

9. SPARE PARTS LIST-7

Part Number	Description	Location(s)
271071361101	RES;360 ,1/16W,1% ,0603,SMT	R56
271071453111	RES;4.53K,1/16W,1% ,0603,SMT	PR25
271013478301	RES;4.7 ,1/4W,5% ,1206,SMT	L31,R21,R24
271002472301	RES;4.7K ,1/10W,5% ,0805,SMT	PR9
271071472302	RES;4.7K ,1/16W,5% ,0603,SMT	PR67,PR7,R106,R111,R1
271071499171	RES;4.99K,1/16W,0.1%,0603,SMT	PR60
271071470301	RES;47 ,1/16W,5% ,0603,SMT	PR51,R510,R511,R564,R
271071471302	RES;470 ,1/16W,5% ,0603,SMT	R212,R525,R530,R533,R
271071474301	RES;470K ,1/16W,5% ,0603,SMT	PR15,R188,R579,R7
271071473101	RES;47K ,1/16W,1% ,0603,SMT	PR508,PR53
271071473301	RES;47K ,1/16W,5% ,0603,SMT	R105,R65,R77
271071499811	RES;49.9 ,1/16W,1% ,0603,SMT	R256,R259
271071562301	RES;5.6K ,1/16W,5% ,0603,SMT	R189,R616,R98
271071565301	RES;5.6M ,1/16W,5% ,0603,SMT	PR52
271071510301	RES;51 ,1/16W,5% ,0603,SMT	R6
271071511102	RES;510 ,1/16W,1% ,0603,SMT	PR77
271071511301	RES;510 ,1/16W,5% ,0603,SMT	R541
271071564301	RES;560K ,1/16W,5% ,0603,SMT	R19,R23
271071576311	RES;576K ,1/16W,1% ,0603,SMT	R203
271071619111	RES;6.19K,1/16W,1% ,0603,SMT	PR57
271071682101	RES;6.8K ,1/16W,1% ,0603,SMT	R62
271071682301	RES;6.8K ,1/16W,5% ,0603,SMT	R502,R503,R504,R505,R
271071619811	RES;61.9 ,1/16W,1% ,0603,SMT	R176
271071681301	RES;680 ,1/16W,5% ,0603,SMT	R513,R242,R243,R244,R
271071715311	RES;715K,1/16W,1%,0603,SMT	PR19

Part Number	Description	Location(s)
271071750101	RES;75 ,1/16W,1% ,0603,SMT	R12,R13,R14,R15,R536,R
271071822301	RES;8.2K ,1/16W,5% ,0603,SMT	R177,R588
271071909101	RES;9.09K,1/16W,1% ,0603,SMT	PR41
271071976111	RES;9.76K,1/16W,1% ,0603,SMT	PR46
271071976311	RES;976K ,1/16W,1% ,0603,SMT	R202
561567009001	REVISED PAGE;GN,7521,NO.1	
271611000301	RP;0*4 ,8P ,1/16W,5% ,0612,SMT	FA5
271571000301	RP;0*8 ,16P ,1/16W,5% ,1606,SMT	RP27,RP28,RP29,RP45,R
271611100301	RP;10*4 ,8P ,1/16W,5% ,0612,SMT	RP40
271571100301	RP;10*8 ,16P ,1/16W,5% ,1606,SMT	RP20,RP22,RP23,RP25,R
271611103301	RP;10K*4 ,8P ,1/16W,5% ,0612,SMT	RP10,RP13,RP39,RP61,R
271621103303	RP;10K*8 ,10P,1/16W,5% ,1206,SMT,TF	RP16,RP18,RP38,RP42,R
271621102303	RP;1K*8 ,10P,1/16W,5% ,1206,SMT,TF	RP35
271621102302	RP;1K*8 ,10P,1/32W,5% ,1206,SMT	RP2
271611220301	RP;22*4 ,8P ,1/16W,5% ,0612,SMT	RP17,RP21,RP24,RP26,R
271611472301	RP;4.7K*4,8P ,1/16W,5% ,0612,SMT	RP1,RP49,RP519,RP6
271621472303	RP;4.7K*8,10P,1/16W,5% ,1206,SMT,TF	RP43,RP524
271621433301	RP;43K*8 ,10P,1/16W,5% ,1206,SMT	RP11,RP12,RP14,RP508,
271621560302	RP;56*4 ,8P ,1/16W,5% ,1206,SMT	RP516
271571560302	RP;56*8 ,16P,1/16W,5% ,1606,SMT	RP3,RP4,RP5,RP501,RP5
271611750301	RP;75*4 ,8P ,1/16W,5% ,0612,SMT	RP15
345666600003	RUBBER;DOWN,LCD,TITAN	
345669600054	RUBBER;HDD_PCBA,RACE	
565167000001	S/W;CD ROM SYSTEM DRIVER,7521	
565180626001	S/W;CD*1,DVD,WIN-DVD,INTERVIDEO	

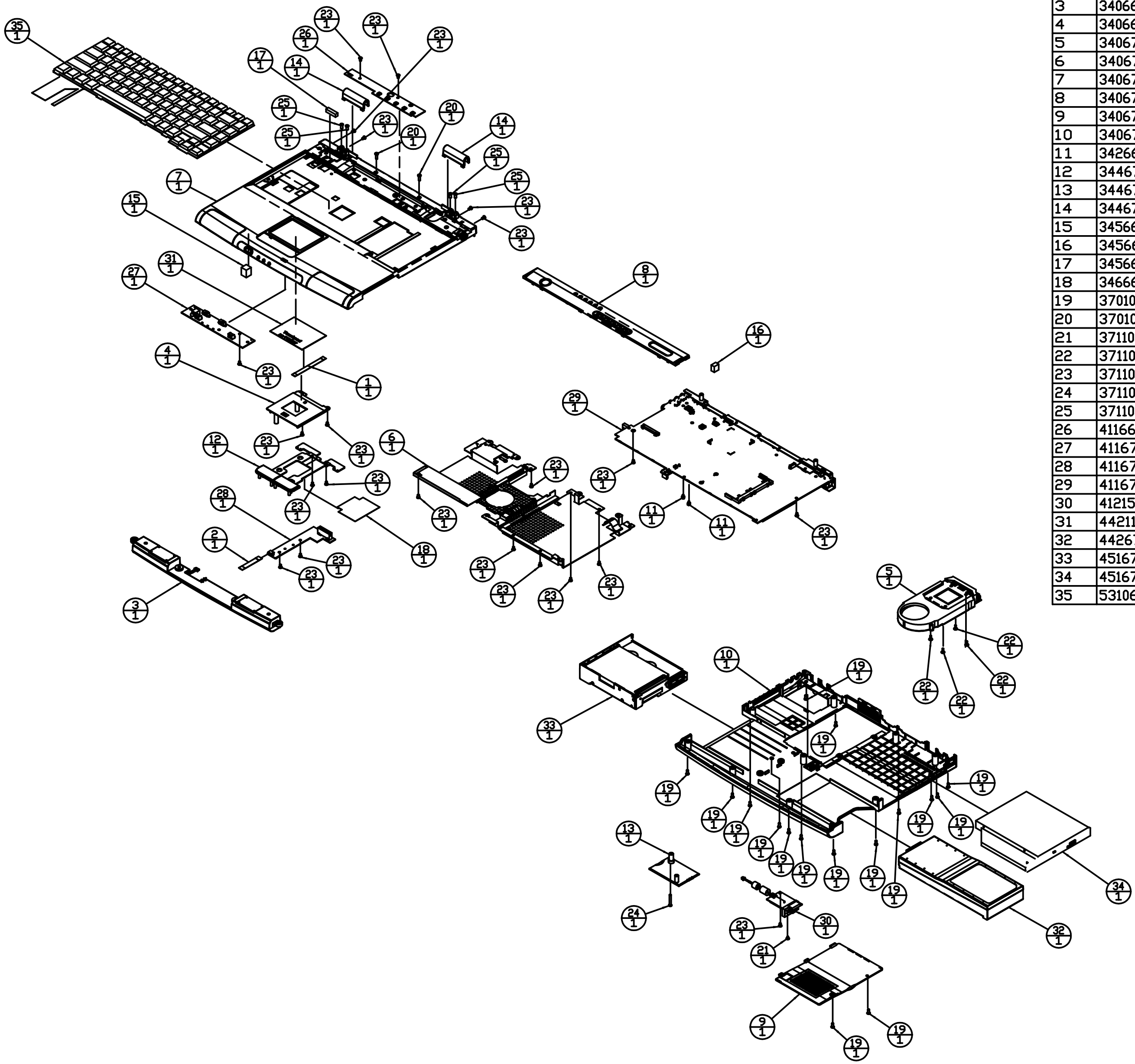
9. SPARE PARTS LIST-8

Part Number	Description	Location(s)
371102030301	SCREW;M2L3,FLT(+),NIB/NLK	
371102030303	SCREW;M2L3,K-HEAD(+),NIW/NLK	
371102030303	SCREW;M2L3,K-HEAD(+),NIW/NLK	
371102030303	SCREW;M2L3,K-HEAD(+),NIW/NLK	
371102030601	SCREW;M2L6,K-HEAD(+),NIB/NLK	
371103030602	SCREW;M3L6,K-HEAD(+),NIB/NLK	
340669600019	SHELDING ASSY;HDD,RACE	
340669600016	SHIELDING ASSY;AUDIO,RACE	
340670020010	SHIELDING ASSY;BOTTOM,7521P	
340669600015	SHIELDING ASSY;CD ROM,RACE	
346669600046	SHIELDING; MEMORY,RACE	
346669600052	SPACER;HDD/FDD PCB,RACE	
346669600016	SPACER;SOCKET 370,REDSEA	
370102611802	SPC-SCREW;M2.6L18,K-HD,NIB/NLK	
370102610405	SPC-SCREW;M2.6L4,NIW,K-HD,t=0.8,NLK	
370102610405	SPC-SCREW;M2.6L4,NIW,K-HD,t=0.8,NLK	
370102610405	SPC-SCREW;M2.6L4,NIW,K-HD,t=0.8,NLK	
370102610603	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	
370102610603	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	
370102610804	SPC-SCREW;M2.6L8,K-HD,t=0.8,NIB/NLK	
370102610804	SPC-SCREW;M2.6L8,K-HD,t=0.8,NIB/NLK	
370102010204	SPC-SCREW;M2L2,NIW/NLK,K-HD	
370102010256	SPC-SCREW;M2L2.5,K-HD(t0.5) NLK,NIW	
370102010253	SPC-SCREW;M2L2.5,NIW/NLK,HD07	
370102020301	SPC-SCREW;M2L3,NIW,K-HEAD	

Part Number	Description	Location(s)
370102010604	SPC-SCREW;M2L6,K-HD(+),NIW/NLK,HEAT	
370103010405	SPC-SCREW;M3L4,NIW,K-HD,T0.3	
340669600003	SPEAKER ASSY;REDSEA	
345669600007	SPOGE; CPU,RACE	
342669600011	STANDOFF;M2DP2H4L5,NIW,RACE	
344669600037	STOPPER;CUP SOCKET,RACE	
297120101005	SW;DIP,SPST,8P,50VDC,.1A,SMT,DHS4S	SW3,SW4
297030105001	SW;PUSH BUTTON,SPSD,48V/.05A,SMT	SW2
297030102001	SW;TOGGLE,SPST,5V/0.2mA,H10.7MM,SMT	SW1
346670000010	THERMAL PAD;HEATSINK,7521	
346669600067	THERMALPAD;M/B,CHOCK,RACE	
346669600006	THERMALPAD;SOCKET,RACE	
340666600018	TILT UNIT;L,TITAN	
340666600017	TILT UNIT;R,TITAN	
340670020011	TOP COVER ASSY;ID3C,7521P	
442164900006	TOUCH PAD MODULE;TM41PUM220-2	
288227002001	TRANS;2N7002LT1,N-CHANNEL FET	PQ1,PQ12,PQ15,PQ16,P
288200144002	TRANS;DTA144WK,PNP,SMT	Q505,Q6
288200144003	TRANS;DTC144TKA,N-MOSFET,SOT-23	Q18,Q5,Q503,Q8,Q9
288200144001	TRANS;DTC144WK,NPN,SOT-23,SMT	PQ6,Q1,Q10,Q13,Q14,Q1
288207811002	TRANS;IRF7811ATR,N-MOS,.01OHM,SO8	PU12,PU19,PU20,PU22,
288202222001	TRANS;MMBT2222AL,NPN,TO236AB	PQ19
288203904010	TRANS;MMBT3904L,NPN,Tr35NS,TO236AB	Q509,Q27
288203906018	TRANS;MMBT3906L,PNP,Tr35NS,TO236AB	Q16
288207002001	TRANS;NDC7002N,N-MOSFET,SSOT-6	PQ21

9. SPARE PARTS LIST-9

Part Number	Description	Location(s)
288202301001	TRANS;SI2301DS,P-MOSFET,SOT-23	PQ17,PQ501,Q21,Q22,Q5
288202302001	TRANS;SI2302DS,N-MOSFET,SOT-23	PQ10,PQ13
288204416001	TRANS;Si4416DY,N-MOSFET,.028OHM,SO8	PQ3,PQ502,PQ504,PQ7
288204435001	TRANS;SI4435DY,P-MOSFET,.035OHM,SO8	PQ22,PU2,PU9
288204832001	TRANS;SI4832DY,N-MOSFET,.028OHM,SO8	PQ503,9
288204920001	TRANS;SI4920DY,NCH-DUAL,5.8A30V,SO8	PU4,PU5
288204925001	TRANS;SI4925DY,P-MOSFET,SO-8	PU16
288209410001	TRANS;SI9410DY,N-MOSFET,.04OHM,SO-8	Q2
273001050022	TRANSFORMER;10/100 BASE,PH163112SMT	U502
373201710550	T-SCREW;P,M1.7L5.5,K-HD(+),0,NIW	
271911103902	VR;10K ,20%,.05W,XV0102GPH1N-9391	VR501
346669600015	WASHER;INVERTER,REDSEA	
421670020002	WIRE ASSY;INVERTER,LCD,7521P	
421670020003	WIRE ASSY;LCD,CHIMEI,7521P	
274011431408	XTAL;14.318M,50PPM,32PF,7*5,4P,SMT	X3
274011431409	XTAL;14.318MHZ,16PF,50PPM,8*4.5,2P	X1
274011600407	XTAL;16MHZ,30PPM,16PF,7*5,4P,SMT	X2
274013276103	XTAL;32.768KHZ,20PPM,12.5PF,CM200	X4



ITEM	PART NO	DESCRIPTION	Q'TY	TYPE	REMARK
1	332669600001	CABLE;FFC,TOUCHPAD,REDSEA	1	PART	IN
2	332669600002	CABLE;FFC,IQSB BD,CHARGER BD,REDSEA	1	PART	IN
3	340669600003	SPEAKER ASSY;REDSEA	1	ASSEMBLY	OUT
4	340669600004	PLATE ASSY;TOUCHOAD,REDSEA	1	ASSEMBLY	IN
5	340670020007	HEATSINK ASSY;CPU,7521p	1	ASSEMBLY	OUT
6	340670020010	SHIELDING ASSY;BOTTOM,7521P	1	ASSEMBLY	0.000
7	340670800003	COVER ASSY;7521N	1	ASSEMBLY	0.000
8	340670800005	COVER ASSY;EASY START,7521N	1	ASSEMBLY	0.000
9	340670800008	COVER ASSY;CPU,7521N	1	ASSEMBLY	0.000
10	340670800010	HOUSING ASSY;TV-OUT,7521N	1	ASSEMBLY	0.000
11	342668700003	STAND-OFF; MODEM,7120	2	PART	
12	344670800013	BUTTON;TOUCH PAD,COVER,7521N	1	PART	
13	344670800015	COVER;MODEM,7521N	1	PART	IN
14	344670800032	COVER;HINGE,7521N	2	PART	IN
15	345669600029	GASKET;COVER,RACE	1	PART	IN
16	345669600041	GASKET;LVDS,9X6X10,RACE	1	PART	IN
17	345669600043	GASKET;MIC,5X5X19,RACE	1	PART	IN
18	346669600039	INSULATOR;TP BUTTON,RACE	1	PART	IN
19	370102610603	SPC-SCREW; M2.6L6 K-HEAD,NIB/NLK	16	PART	
20	370102610801	SPC-SCREW;M2.6L8,NIB	2	PART	IN
21	371102030303	SPC-SCREW; M2L3 K-HEAD,NIW	1	PART	IN
22	371102030601	SCREW; M2L6 K-HEAD,NIB,NIW	4	PART	IN
23	371102610405	SPC-SCREW; M2.6L4 K-HEAD,NIB	22	PART	IN
24	371102611802	SPC-SCREW; M2.6L18 K-HEAD,NIB	1	PART	IN
25	371103030602	SPC-SCREW; M3L6 K-HEAD,NIB	4	PART	
26	411669600007	PWA;PWA-REDSEA,QSB TRANS BD,SMT	1	ASSEMBLY	OUT
27	411670000010	PWA;PWA-7521,IQSB TRANS BD,T/U	1	ASSEMBLY	OUT
28	411670000031	PWA;PWA-7521,CHARGE TRANS BD	1	ASSEMBLY	OUT
29	411670800001	PWA;PWA-7521N-ENS,128M,MOTHER BD	1	ASSEMBLY	0.000
30	412155600049	PCB ASSY;MDM,56K,UNIV,W/Z Y-CAP,	1	ASSEMBLY	OUT
31	442110500009	TOUCH PAD MODULE;90425	1	PART	OUT
32	442670800001	BATT ASSY;10.8V,4.5AH,NI,SYO,752	1	ASSEMBLY	0.000
33	451670800003	HDD ME KIT;7521N	1	ASSEMBLY	0.000
34	451670800004	CD-ROM ME KIT;24X,224E-A92,7521N	1	ASSEMBLY	0.000
35	5310670800001	KBD ASSY;US,W/EMI,7521N	1	ASSEMBLY	OUT

TOL± RANGE	M1	M2	S1	S2	P1	P2	C	B
0~6	.05	0.1	.15	0.2	.05	0.1	0.5	.15
6~30	0.1	0.2	.15	.25	0.1	.15	1	.15
30~80	.15	.25	0.2	0.3	0.2	0.4	2	.25
80~180	.15	0.3	.25	.45	0.4	0.8	3	.25
180~315	0.2	0.5	0.4	0.6	0.6	1.2	3	0.3
315~800	0.3	0.8	0.7	1.1	0.8	1.5	4	0.5

ITEM | CONTENTS OF CHANGE | RVS | CHK | APV | M/D/Y

DATE 06-Aug-01 | MATERIAL SEE NOTES | TREATMENT | REMARK

UNIT MM | SCALE 0.30 | DRAWING NAME HOUSING;KIT,7521N

DRAWN | DESIGNED | CHECKED | APPROVED | MATERIAL NO. MF 451670800007 R00

MiTAC Technology Corp.

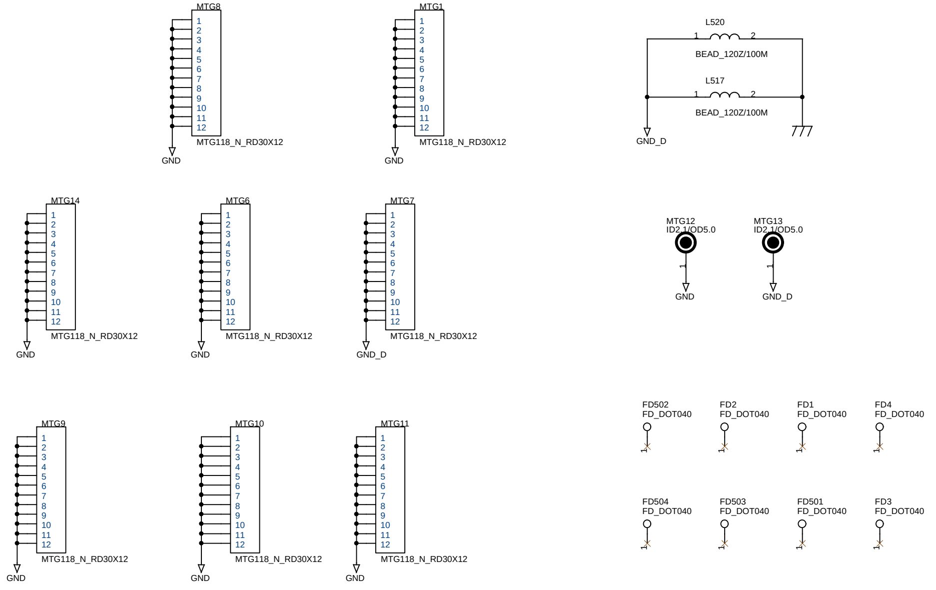
model name7521-NEC-STRUCTURAL

file nameHOUSING-KIT-7521N

SHEET NO. 1 of 1

7521 plus R02

REV	DESCRIPTION OF CHANGE	ECR	DATE	APPROVAL
R00			09/29/2000	
R0B	1.Add 10K ohm pull high resistor between +3v and DS90363 pin 14. 2.Add frequency select resistor. 3.Add ESD solution on PCMCIA socket. 4.Change test pin resistor of SiS900 form 4.7K to 10K ohm. 5.Correct autoload pin of SiS900 power form +5V to +S5V. 6.Add 0 ohm pull high resistor between +S5V and EEPROM pin 6. 7.Modify Vcc_RTC circuit. 8.Modify Vmain_PWROK circuit. 9.Modify Vcc_CORE circuit. 10.Change SiS900 interrupt from IRQB to IRQC. 12.Add filter circuit for 25Mhz oscillator.		02/01/2001	
R01	1.Add RLZ5.6B between VDD5 to GND. 2.Modify GPIO 83601R reset circiut. 3.Modify CH7005 R-set circiut. 4.Add LCD panel ID select DIP switch. 5.Modify CRT_ISOLATE circuit. 6.Modify LM393A circuit for RTC data loss problem.		03/01/2001	
R02	1.Add AGPAVDD1 circiut for LCD panel incorrect color. 2.Modify "Enable_VGA AND PCI_RST#" circuit.		04/30/2001	

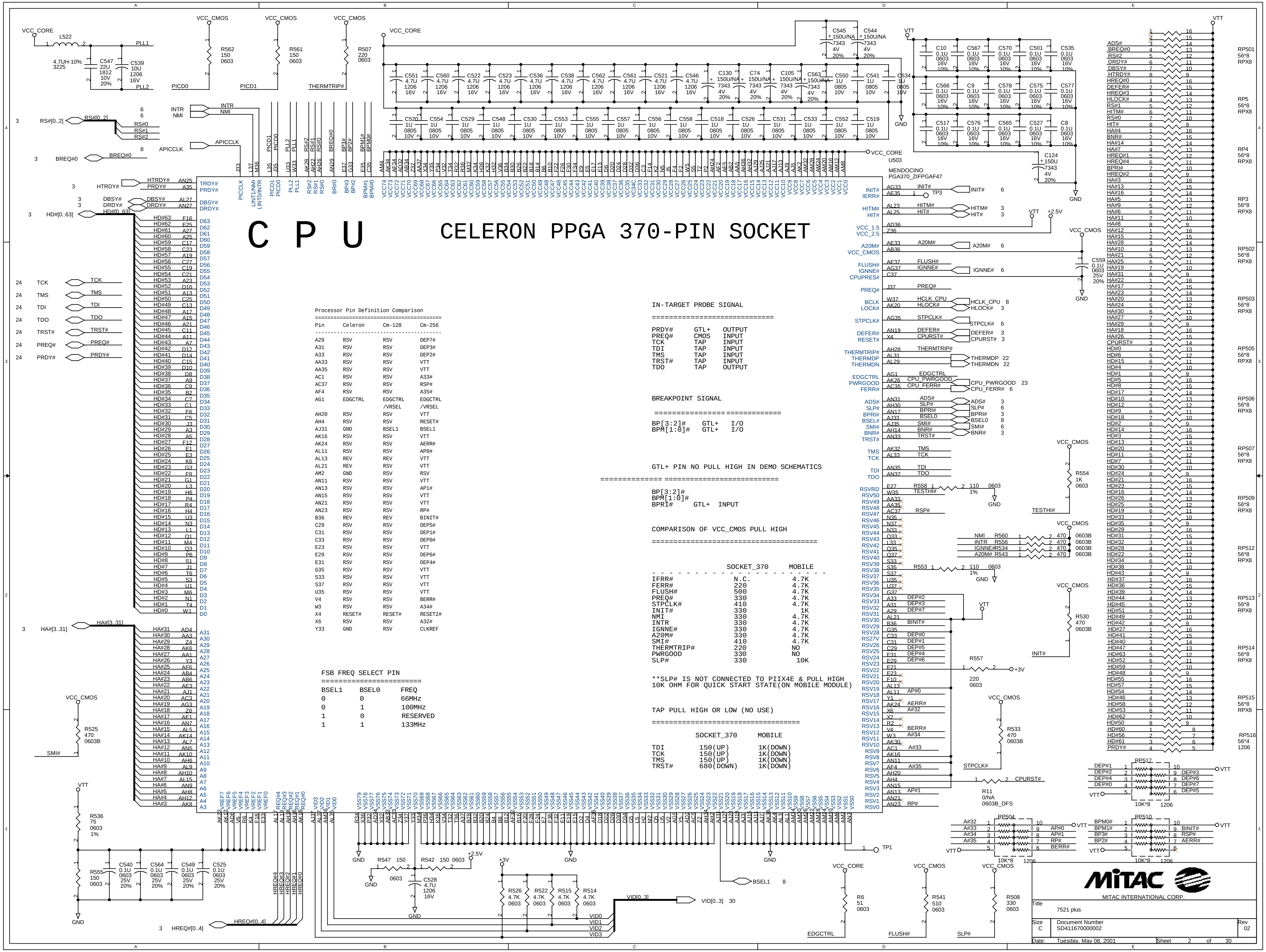


DRAWN	DESIGN	CHECK	ISSUES

MITAC

MITAC INTERNATIONAL CORP.

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Processor Pin Definition Comparison

Pin	Celeron	Cm-128	Cm-256
A29	RSV	RSV	DEP7#
A31	RSV	RSV	DEP3#
A33	RSV	RSV	DEP2#
AA33	RSV	RSV	VTT
AA35	RSV	RSV	VTT
AC1	RSV	RSV	A33#
AC37	RSV	RSV	RSP#
AF4	RSV	RSV	A35#
AG1	EDGCTRL	EDGCTRL /VRSEL	EDGCTRL /VRSEL
AH20	RSV	RSV	VTT
AH4	RSV	RSV	RESET#
AJ31	GND	BSEL1	BSEL1
AK16	RSV	RSV	VTT
AK24	RSV	RSV	AERR#
AL11	RSV	RSV	AP0#
AL13	REV	REV	VTT
AL21	REV	RSV	VTT
AM2	GND	RSV	RSV
AN11	RSV	RSV	VTT
AN13	RSV	RSV	AP1#
AN15	RSV	RSV	VTT
AN21	RSV	RSV	VTT
AN23	RSV	RSV	RP#
B36	REV	REV	BINIT#
C29	RSV	RSV	DEP5#
C31	RSV	RSV	DEP1#
C33	RSV	RSV	DEP0#
E23	RSV	RSV	VTT
E29	RSV	RSV	DEP6#
E31	RSV	RSV	DEP4#
G35	RSV	RSV	VTT
S33	RSV	RSV	VTT
S37	RSV	RSV	VTT
U35	RSV	RSV	VTT
V4	RSV	RSV	BERR#
W3	RSV	RSV	A34#
X4	RESET#	RESET#	RESET2#
X6	RSV	RSV	A32#
Y33	GND	RSV	CLKREF

FSB FREQ SELECT PIN

BSEL1	BSEL0	FREQ
0	0	66MHz
0	1	100MHz
1	0	RESERVED
1	1	133MHz

IN-TARGET PROBE SIGNAL

PRDY#	GTL+	OUTPUT
PREQ#	CMOS	INPUT
TCK	TAP	INPUT
TDI	TAP	INPUT
TMS	TAP	INPUT
TRST#	TAP	INPUT
TDO	TAP	OUTPUT

BREAKPOINT SIGNAL

BP[3:2]#	GTL+	I/O
BPM[1:0]#	GTL+	I/O

GTL+ PIN NO PULL HIGH IN DEMO SCHEMATICS

BP[3:2]#
BPM[1:0]#
BPRI# GTL+ INPUT

COMPARISON OF VCC_CMOS PULL HIGH

	SOCKET_370	MOBILE
IFRR#	N.C.	4.7K
FERR#	220	4.7K
FLUSH#	500	4.7K
PREQ#	330	4.7K
STPCLK#	410	4.7K
INIT#	330	1K
NMI	330	4.7K
INTR	330	4.7K
IGNNE#	330	4.7K
A20M#	330	4.7K
SMI#	410	4.7K
THERMTRIP#	220	NO
PWRGOOD	330	NO
SLP#	330	10K

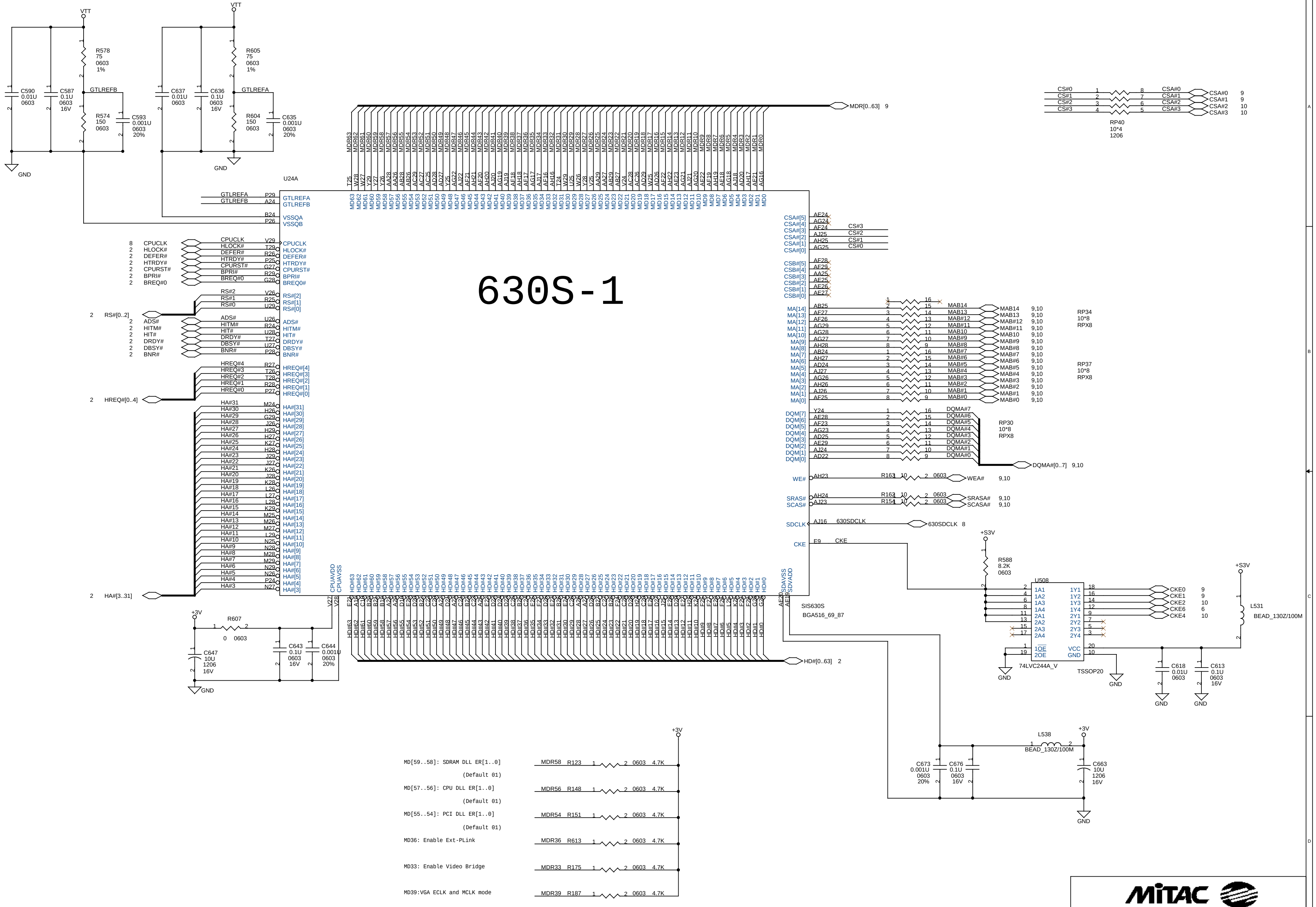
**SLP# IS NOT CONNECTED TO PIIX4E & PULL HIGH 10K OHM FOR QUICK START STATE(ON MOBILE MODULE)

TAP PULL HIGH OR LOW (NO USE)

	SOCKET_370	MOBILE
TDI	150(UP)	1K(DOWN)
TCK	150(UP)	1K(DOWN)
TMS	150(UP)	1K(DOWN)
TRST#	680(DOWN)	1K(DOWN)

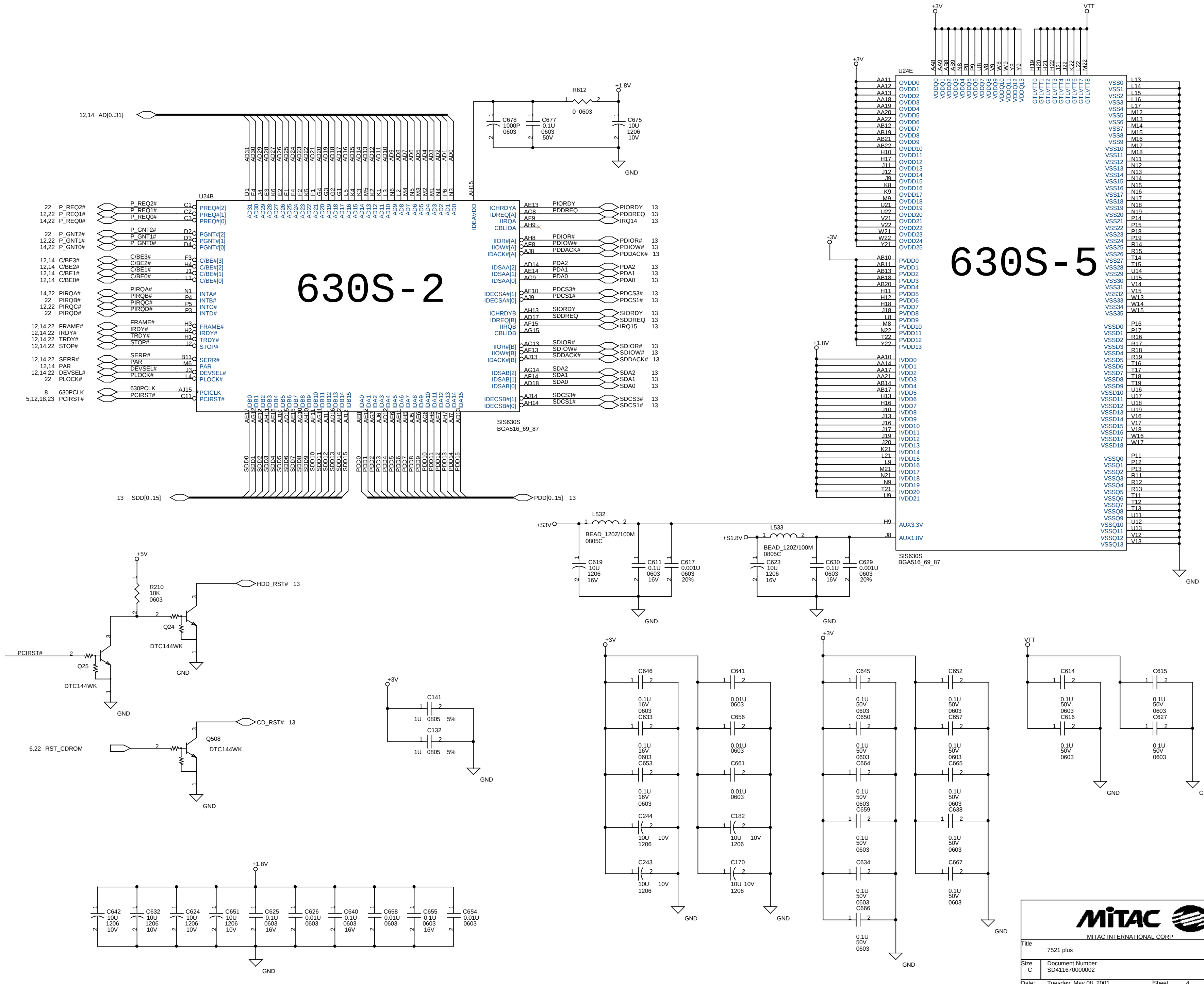
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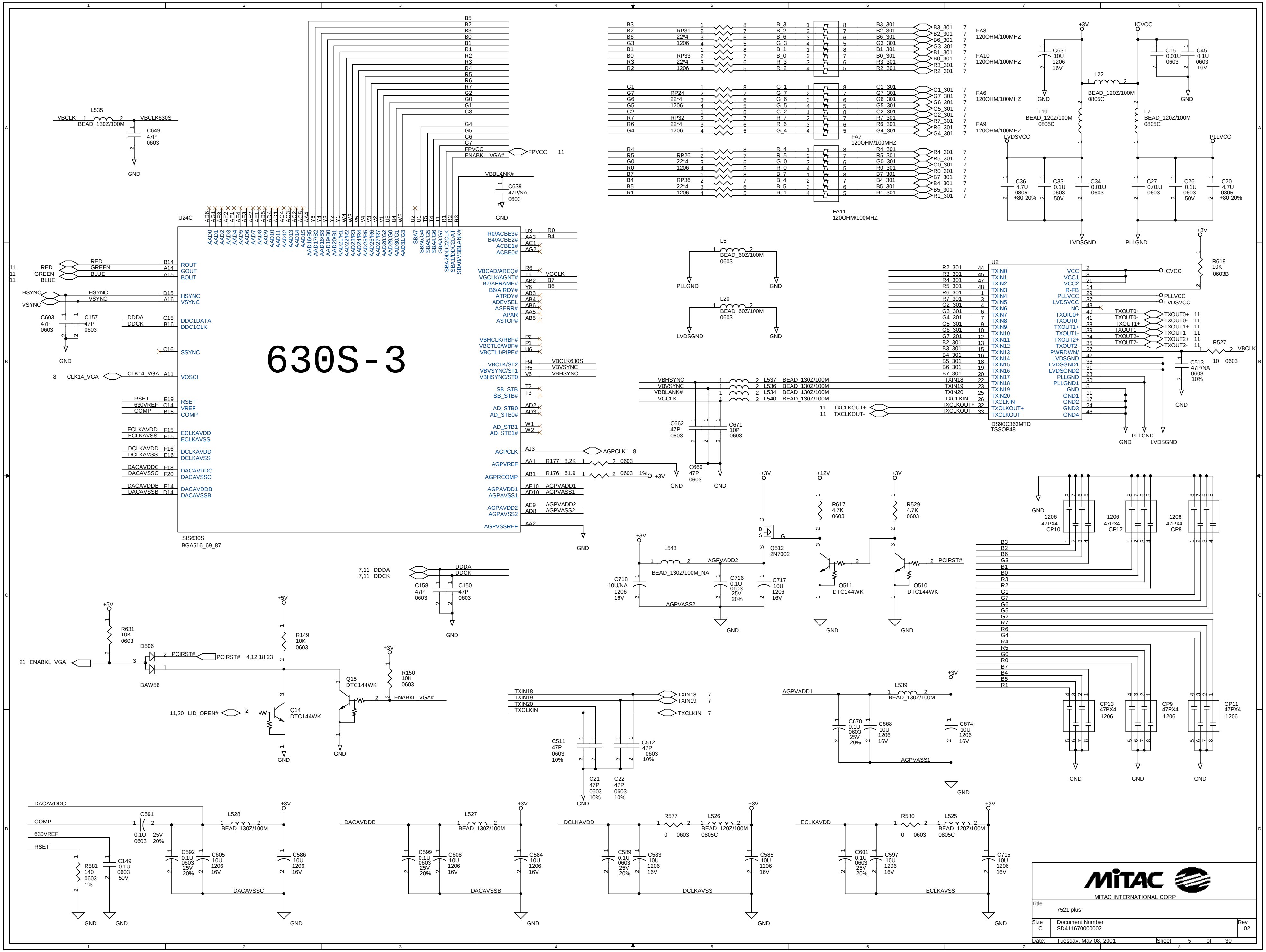
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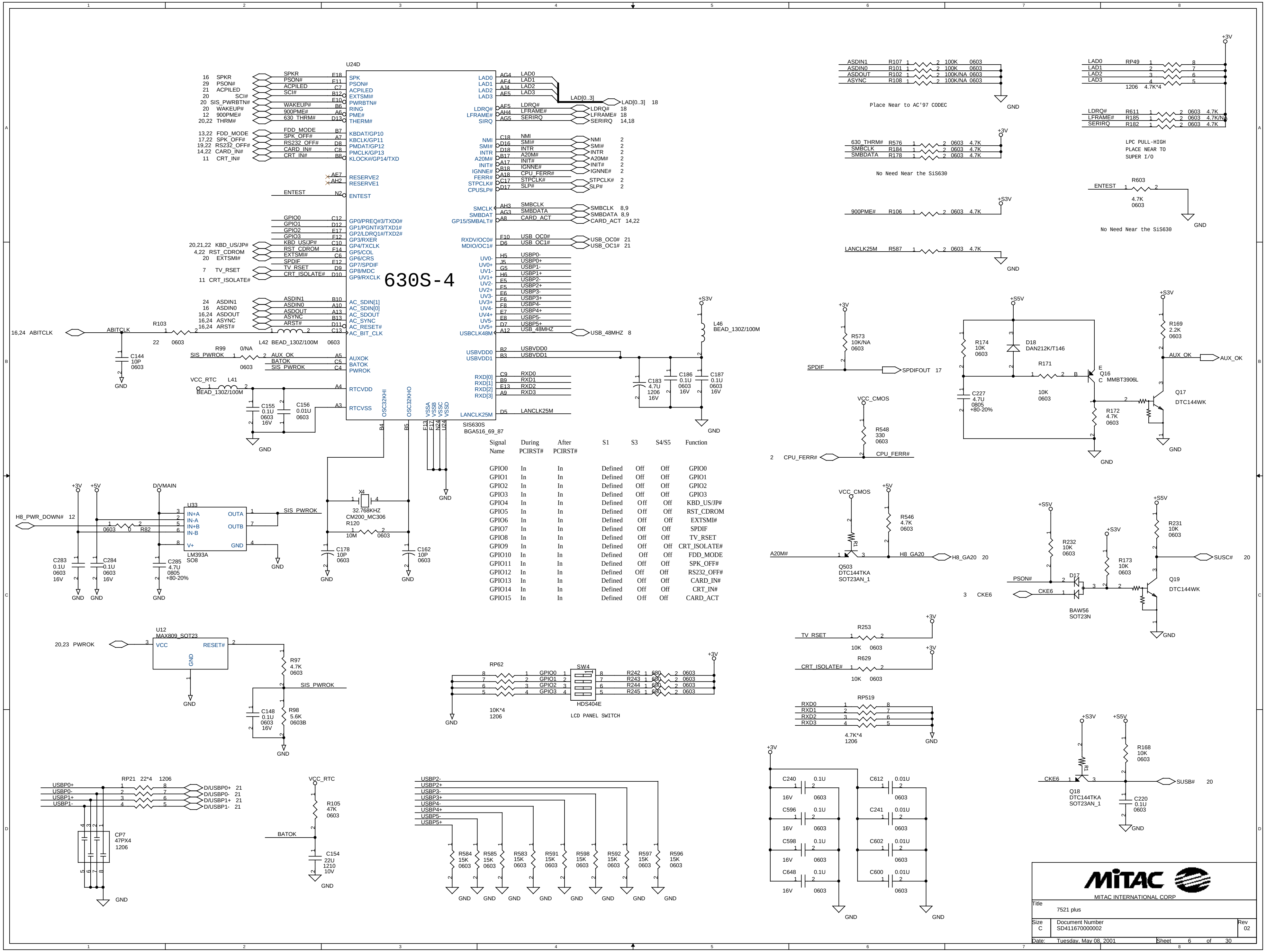


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630S-3
U24C
SIS630S
BGA516_69_87
U2
DS90C363MTD
TSSOP48
L535 BEAD_130Z/100M
VBCLK
VBCLK630S
C649 47P 0603
GND
RED GREEN BLUE
HSYNC VSYNC
DDDA DDCK
CLK14_VGA
RSET 630VREF COMP
ECLKAVDD ECLKAVSS
DCLKAVDD DCLKAVSS
DACAVDDC DACAVSSC
DACAVDDB DACAVSSB
AGPCLK
AGPVREF
AGPRCOMP
AGPVADD1 AGPVASS1
AGPVADD2 AGPVASS2
AGPVSSREF
FPVCC
ENABKL_VGA#
VBBLANK#
C639 47P/NA 0603
RP31 22*4 1206
RP33 22*4 1206
RP24 22*4 1206
RP32 22*4 1206
RP26 22*4 1206
RP36 22*4 1206
FA8 120OHM/100MHZ
FA10 120OHM/100MHZ
FA6 120OHM/100MHZ
FA9 120OHM/100MHZ
FA7 120OHM/100MHZ
FA11 120OHM/100MHZ
L22 BEAD_120Z/100M 0805C
L19 BEAD_120Z/100M 0805C
L7 BEAD_120Z/100M 0805C
ICVCC
LVDSVCC
PLLVCC
LVDSGND
PLLGND
L5 BEAD_60Z/100M 0603
L20 BEAD_60Z/100M 0603
R619 10K 0603B
TXOUT0+ TXOUT0- TXOUT1+ TXOUT1- TXOUT2+ TXOUT2-
TXCLKOUT+ TXCLKOUT-
R527 10 0603
C513 47P/NA 0603 10%
L537 BEAD_130Z/100M
L536 BEAD_130Z/100M
L534 BEAD_130Z/100M
L540 BEAD_130Z/100M
VBHSYNC VBVSYNC VBBLANK# VGCLK
C662 47P 0603
C671 10P 0603
C660 47P 0603
L543 BEAD_130Z/100M_NA
C718 10U/NA 1206 16V
C716 0.1U 0603 25V 20%
C717 10U 1206 16V
Q512 2N7002
R617 4.7K 0603
Q511 DTC144WK
R529 4.7K 0603
Q510 DTC144WK
PCIRST#
CP10 47PX4 1206
CP12 47PX4 1206
CP8 47PX4 1206
CP13 47PX4 1206
CP9 47PX4 1206
CP11 47PX4 1206
C158 47P 0603
C150 47P 0603
R631 10K 0603
D506 BAW56
ENABKL_VGA
PCIRST# 4,12,18,23
R149 10K 0603
Q14 DTC144WK
Q15 DTC144WK
R150 10K 0603
LID_OPEN#
TXIN18 TXIN19 TXIN20 TXCLKIN
C511 47P 0603 10%
C512 47P 0603 10%
C21 47P 0603 10%
C22 47P 0603 10%
L539 BEAD_130Z/100M
C670 0.1U 0603 25V 20%
C668 10U 1206 16V
C674 10U 1206 16V
C591 0.1U 0603 25V 20%
R581 140 0603 1%
C149 0.1U 0603 50V
L528 BEAD_130Z/100M
C592 0.1U 0603 25V 20%
C605 10U 1206 16V
C586 10U 1206 16V
L527 BEAD_130Z/100M
C599 0.1U 0603 25V 20%
C608 10U 1206 16V
C584 10U 1206 16V
R577 0 0603
L526 BEAD_120Z/100M 0805C
C589 0.1U 0603 25V 20%
C583 10U 1206 16V
C585 10U 1206 16V
R580 0 0603
L525 BEAD_120Z/100M 0805C
C601 0.1U 0603 25V 20%
C597 10U 1206 16V
C715 10U 1206 16V
MITAC
MITAC INTERNATIONAL CORP
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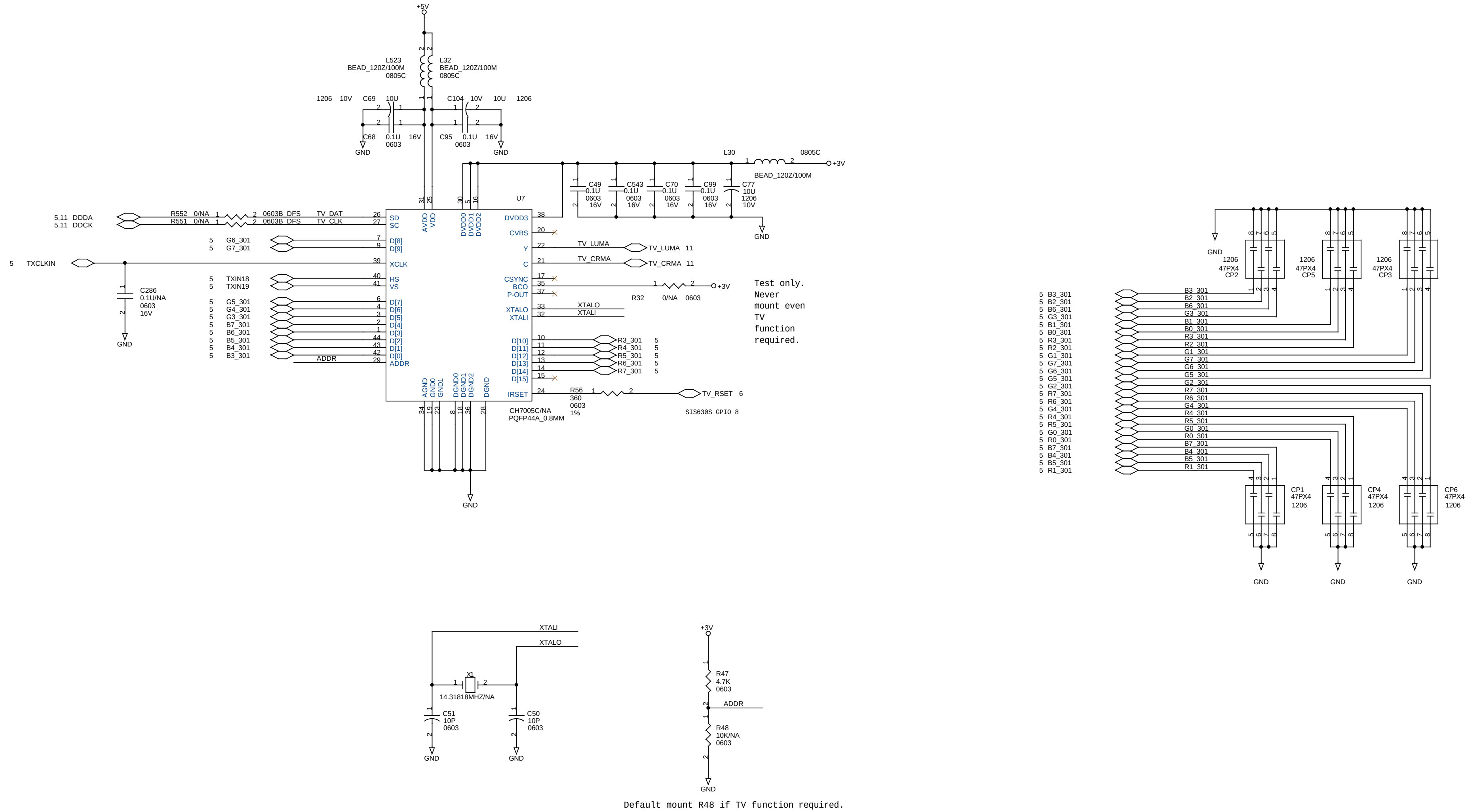
Signal Name	During PCIRST#	After PCIRST#	S1	S3	S4/S5	Function
GPIO0	In	In	Defined	Off	Off	GPIO0
GPIO1	In	In	Defined	Off	Off	GPIO1
GPIO2	In	In	Defined	Off	Off	GPIO2
GPIO3	In	In	Defined	Off	Off	GPIO3
GPIO4	In	In	Defined	Off	Off	KBD_US/JP#
GPIO5	In	In	Defined	Off	Off	RST_CDROM
GPIO6	In	In	Defined	Off	Off	EXTSMI#
GPIO7	In	In	Defined	Off	Off	SPDIF
GPIO8	In	In	Defined	Off	Off	TV_RSET
GPIO9	In	In	Defined	Off	Off	CRT_ISOLATE#
GPIO10	In	In	Defined	Off	Off	FDD_MODE
GPIO11	In	In	Defined	Off	Off	SPK_OFF#
GPIO12	In	In	Defined	Off	Off	RS232_OFF#
GPIO13	In	In	Defined	Off	Off	CARD_IN#
GPIO14	In	In	Defined	Off	Off	CRT_IN#
GPIO15	In	In	Defined	Off	Off	CARD_ACT

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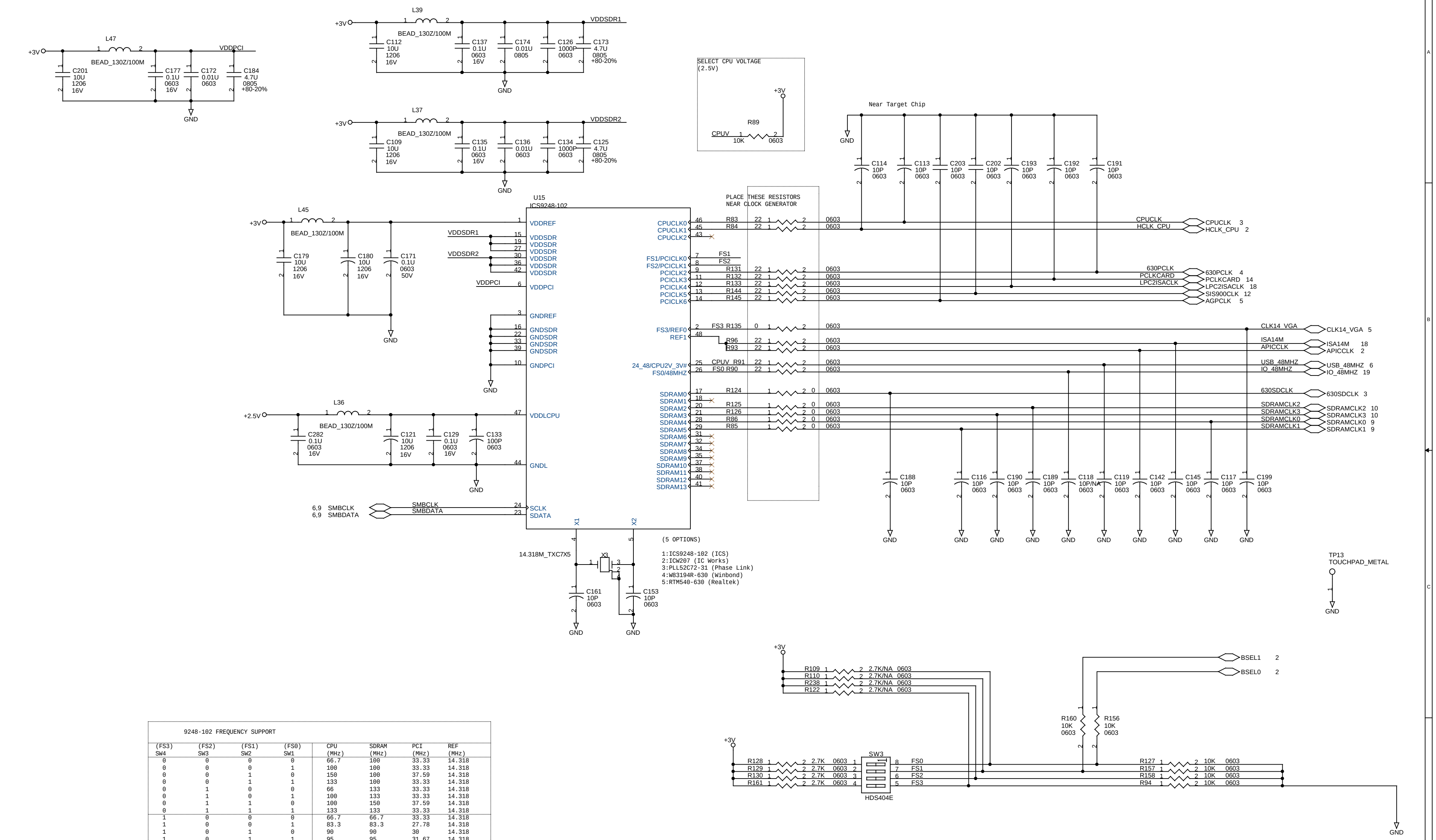
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CLOCK SYNTHESIZER AND DRIVER



9248-102 FREQUENCY SUPPORT

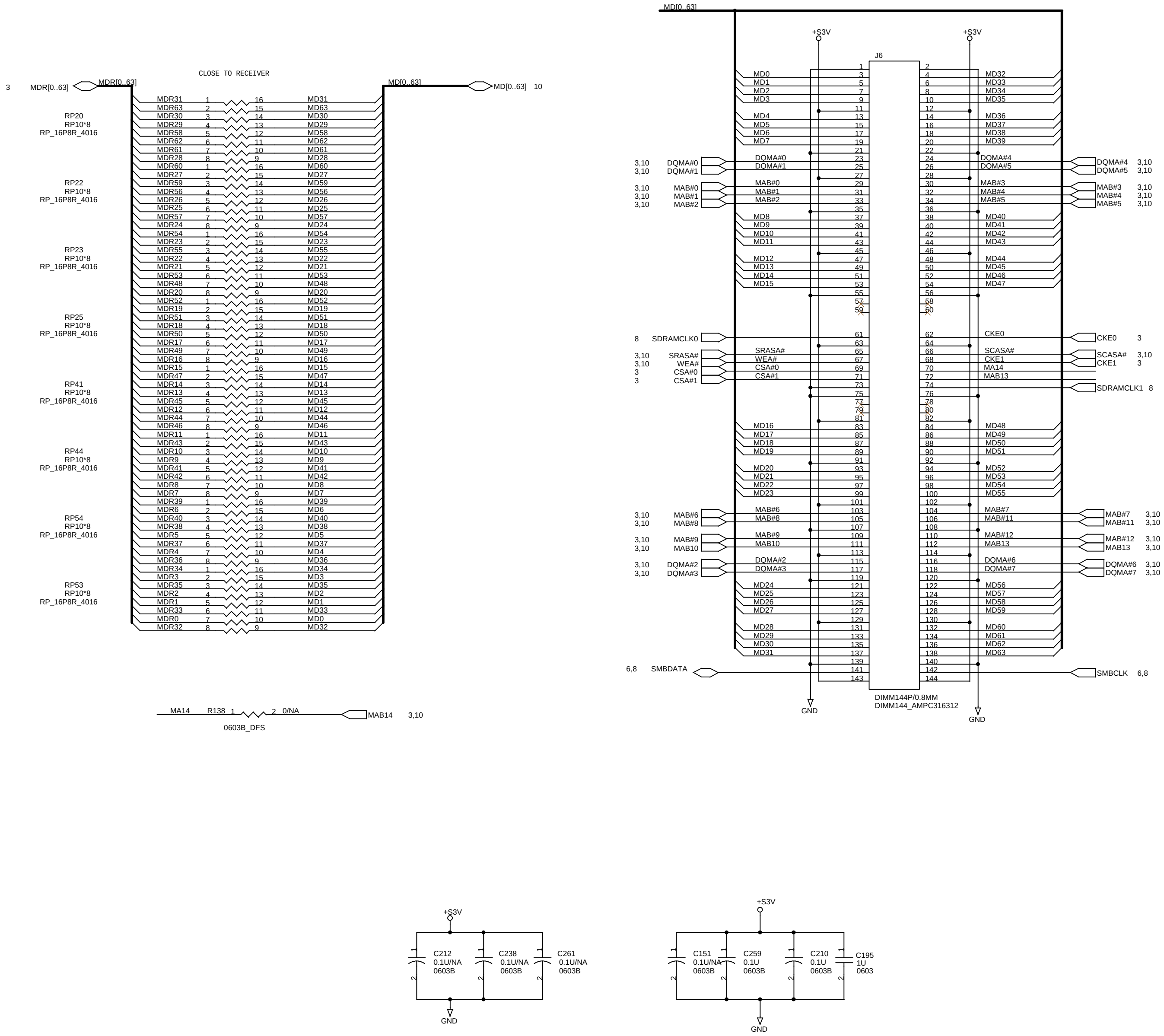
(FS3) SW4	(FS2) SW3	(FS1) SW2	(FS0) SW1	CPU (MHz)	SDRAM (MHz)	PCI (MHz)	REF (MHz)
0	0	0	0	66.7	100	33.33	14.318
0	0	0	1	100	100	33.33	14.318
0	0	1	0	150	100	37.59	14.318
0	0	1	1	133	100	33.33	14.318
0	1	0	0	66	133	33.33	14.318
0	1	0	1	100	133	33.33	14.318
0	1	1	0	100	150	37.59	14.318
0	1	1	1	133	133	33.33	14.318
1	0	0	0	66.7	66.7	33.33	14.318
1	0	0	1	83.3	83.3	27.78	14.318
1	0	1	0	90	90	30	14.318
1	0	1	1	95	95	31.67	14.318
1	1	0	0	95	126.67	31.67	14.318
1	1	0	1	112	112	37.34	14.318
1	1	1	0	166	111	27.67	14.318
1	1	1	1	166	166	27.67	14.318

0:OFF
1:ON

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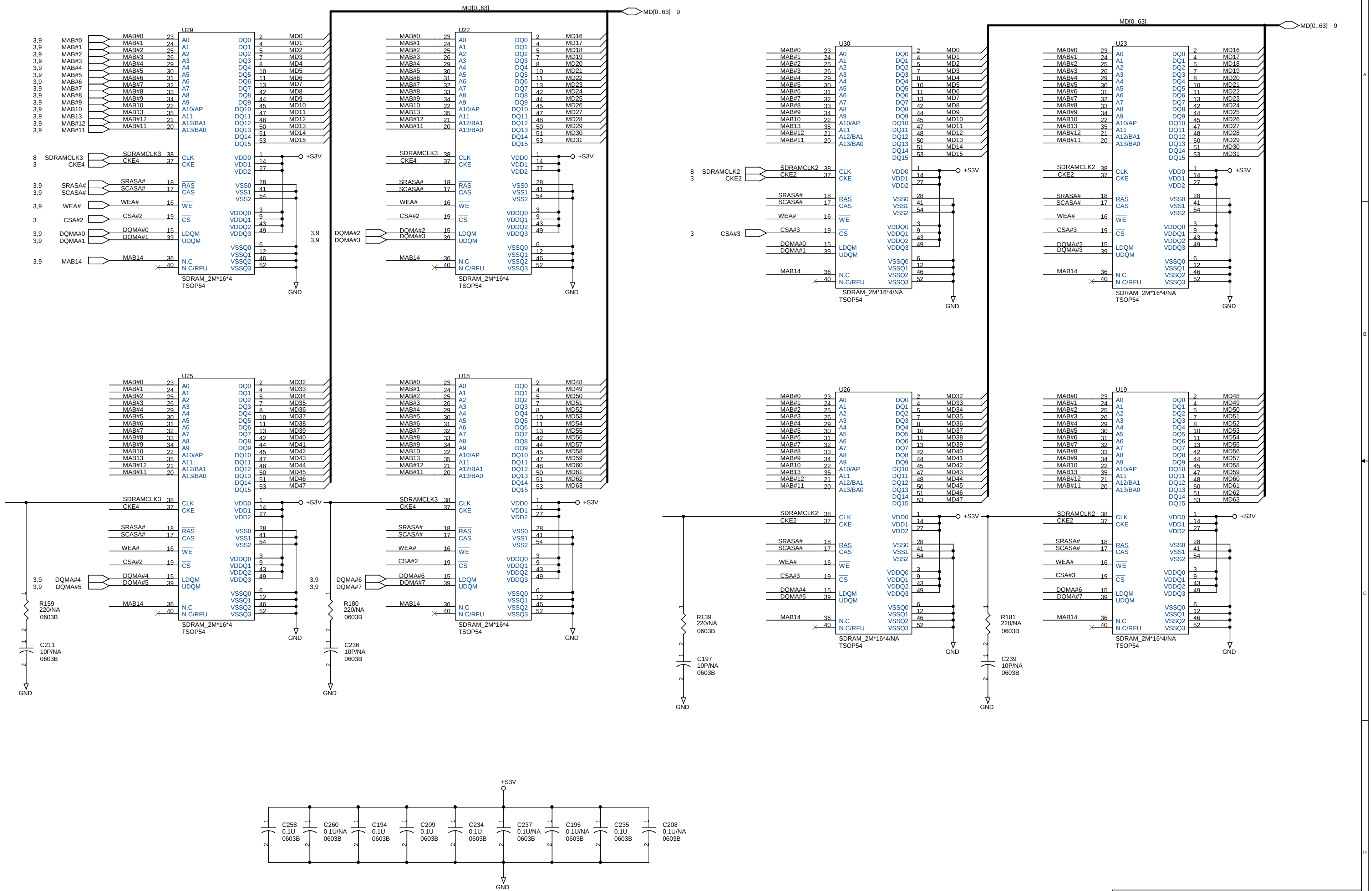
144 PIN SODIMM SOCKET



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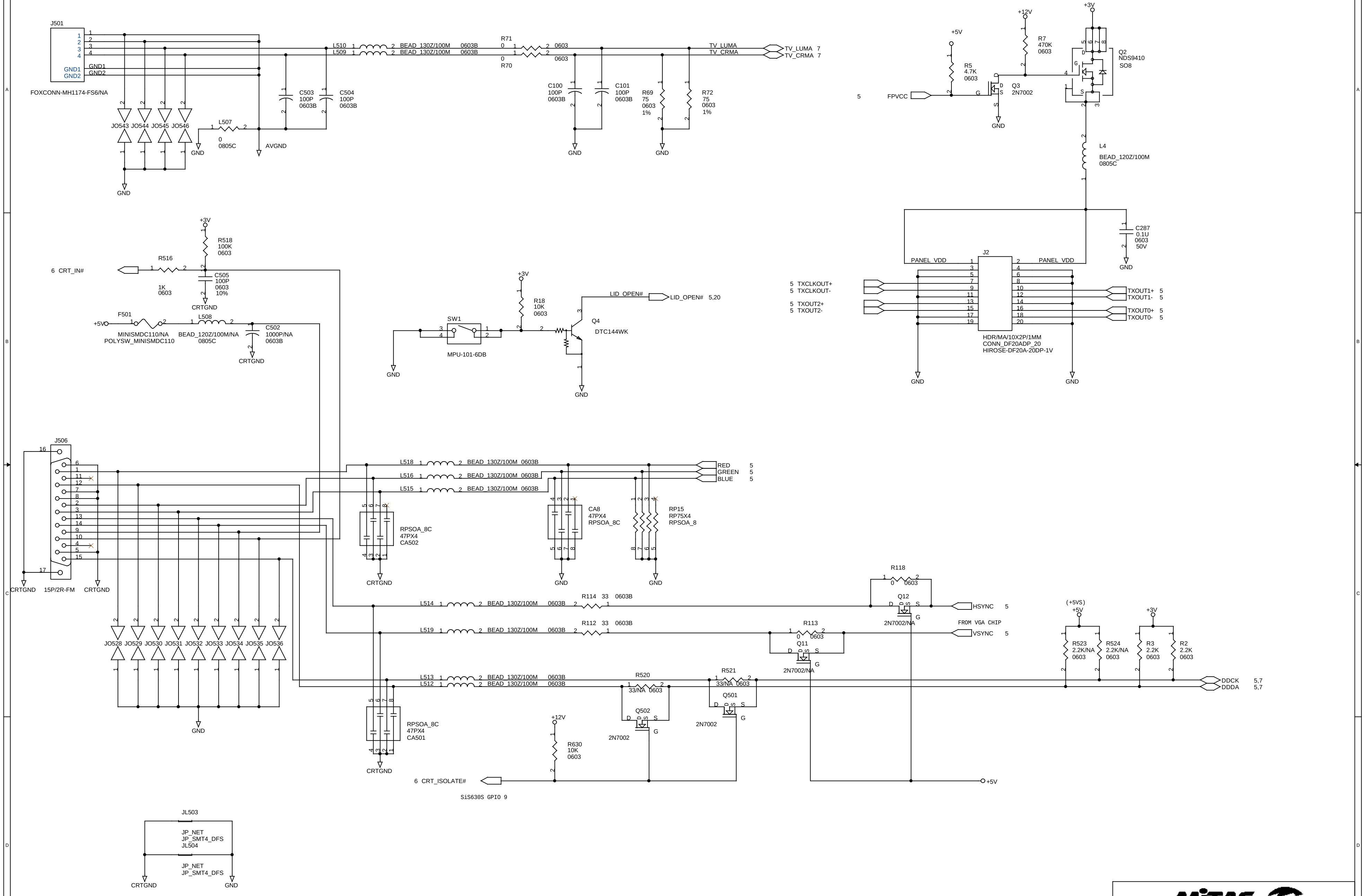
2M X 16 BITS X 4 BANK X 4 = 64M BYTES



MiTAC

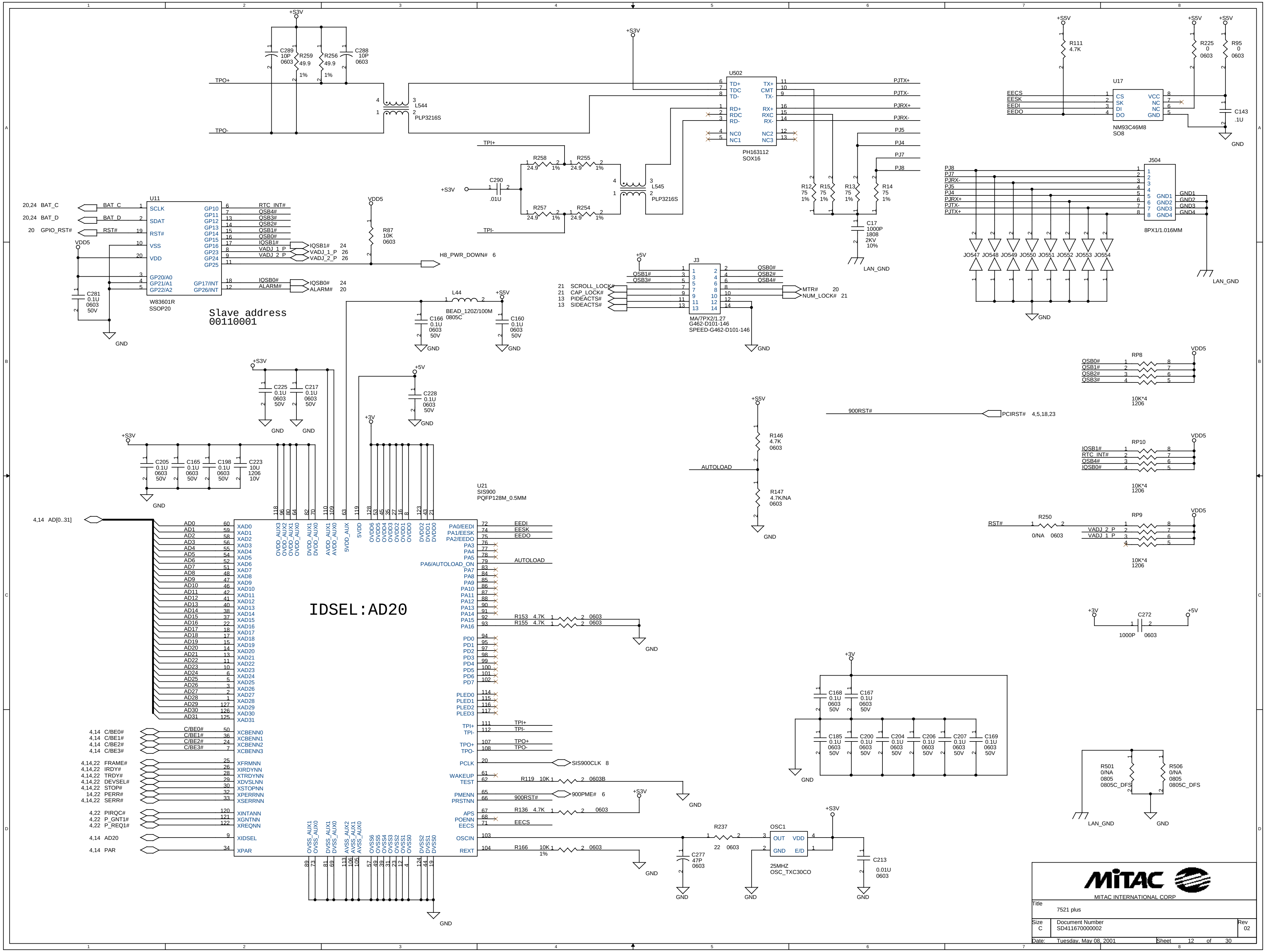
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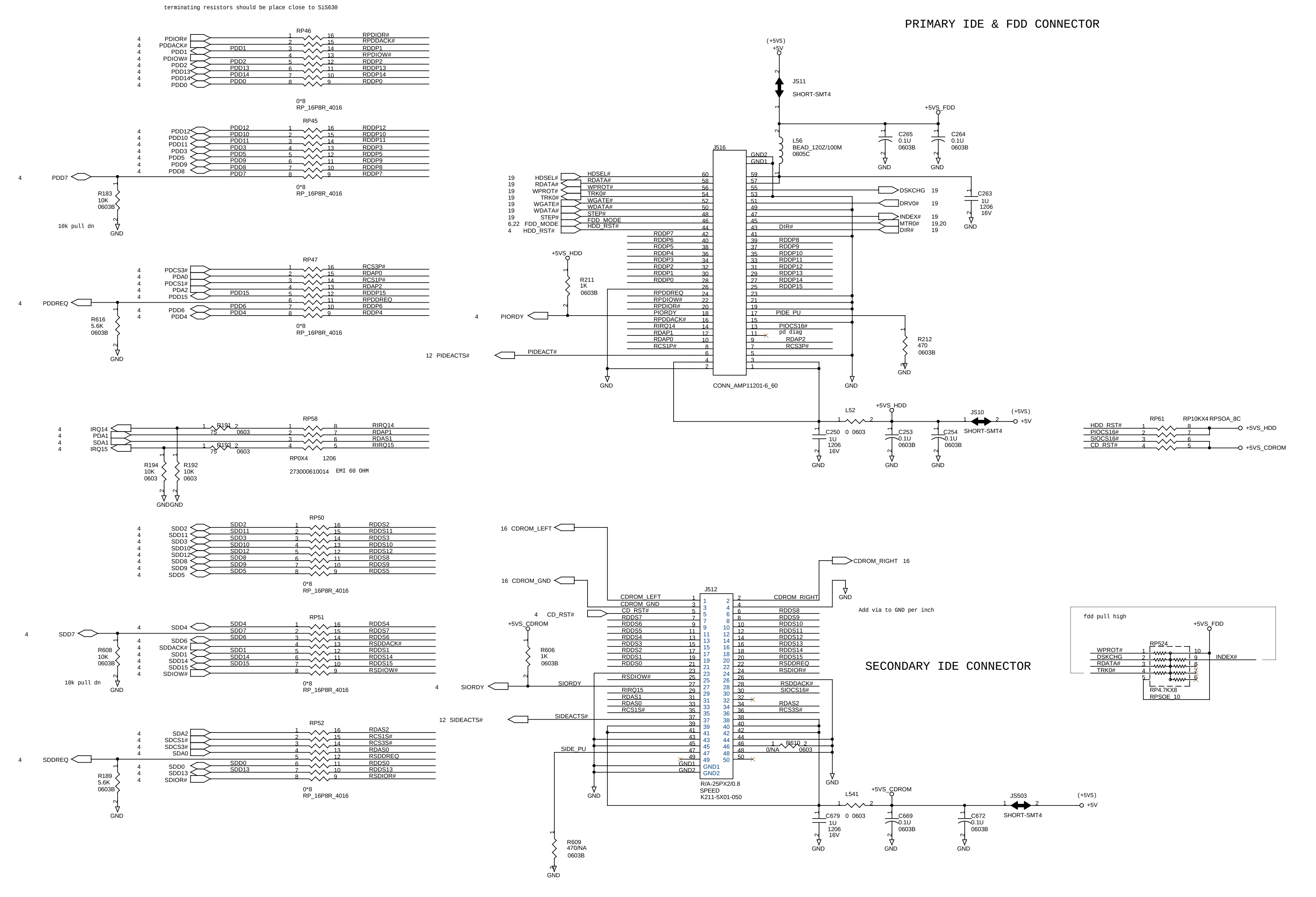
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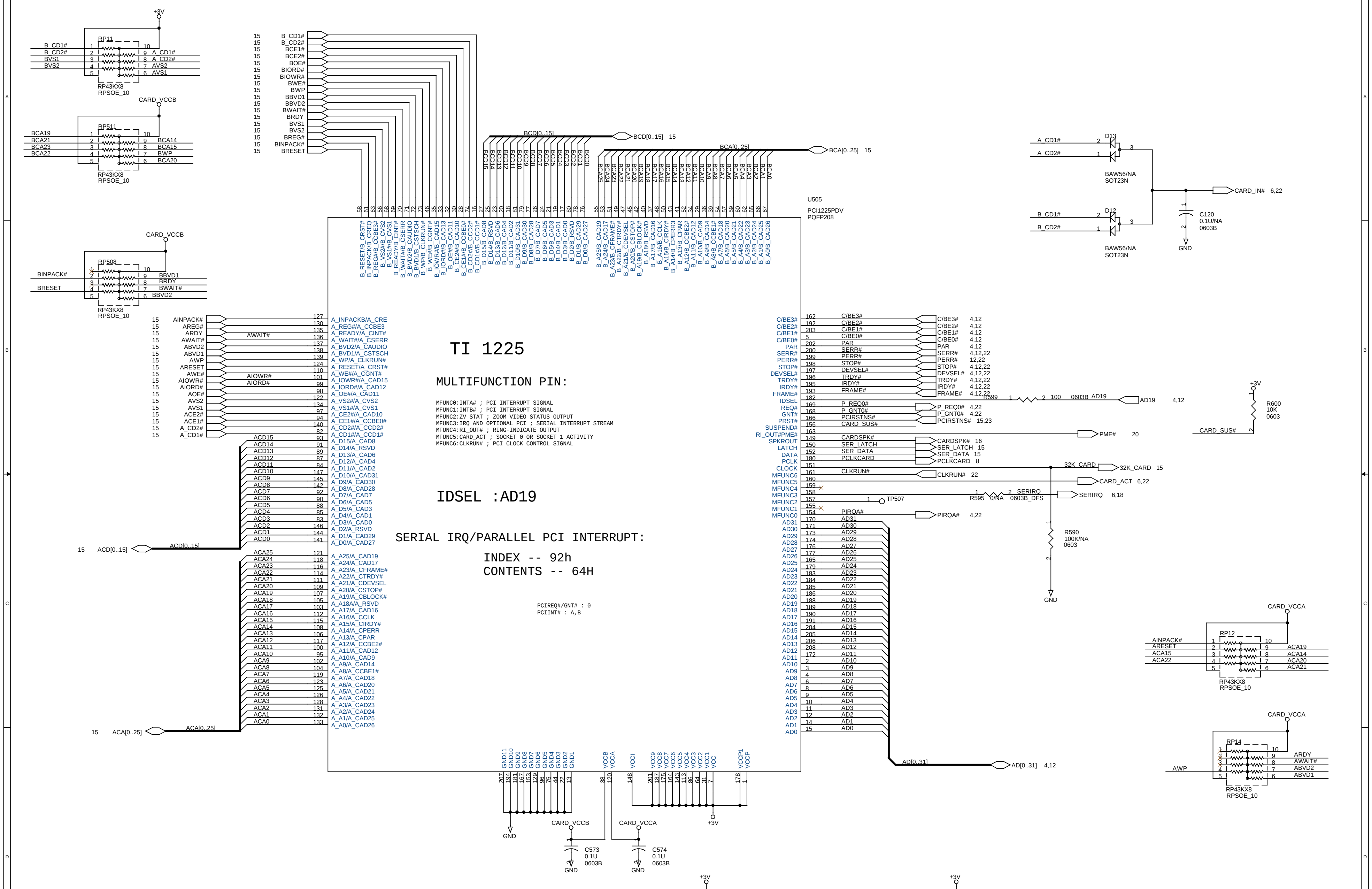
U502
PH163112
SOX16
L544
PLP3216S
L545
PLP3216S
U17
NM93C46M8
SO8
J504
8PX1/1.016MM
U11
W83601R
SSOP20
Slave address
00110001
J3
MA/7PX2/1.27
G462-D101-146
SPEED-G462-D101-146
L44
BEAD_120Z/100M
0805C
RP8
RP9
RP10
10K*4
1206
U21
SIS900
PQFP128M_0.5MM
IDSEL:AD20
OSC1
25MHZ
OSC_TXC30CO
900RST#
PCIRST#
AUTOLOAD
SIS900CLK
900PME#
H8_PWR_DOWN#
LAN_GND
GND
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PRIMARY IDE & FDD CONNECTOR



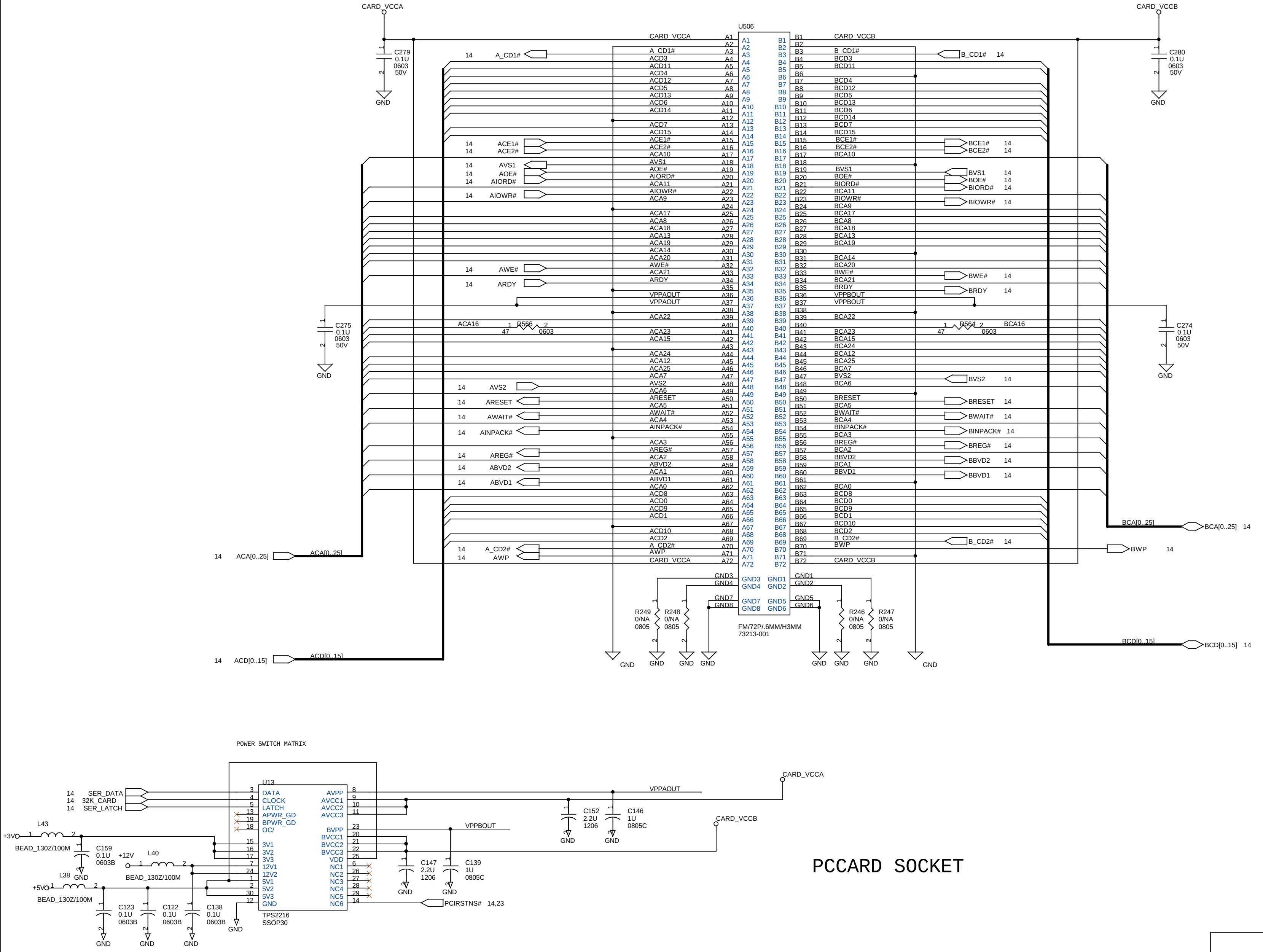
MITAC INTERNATIONAL CORP.

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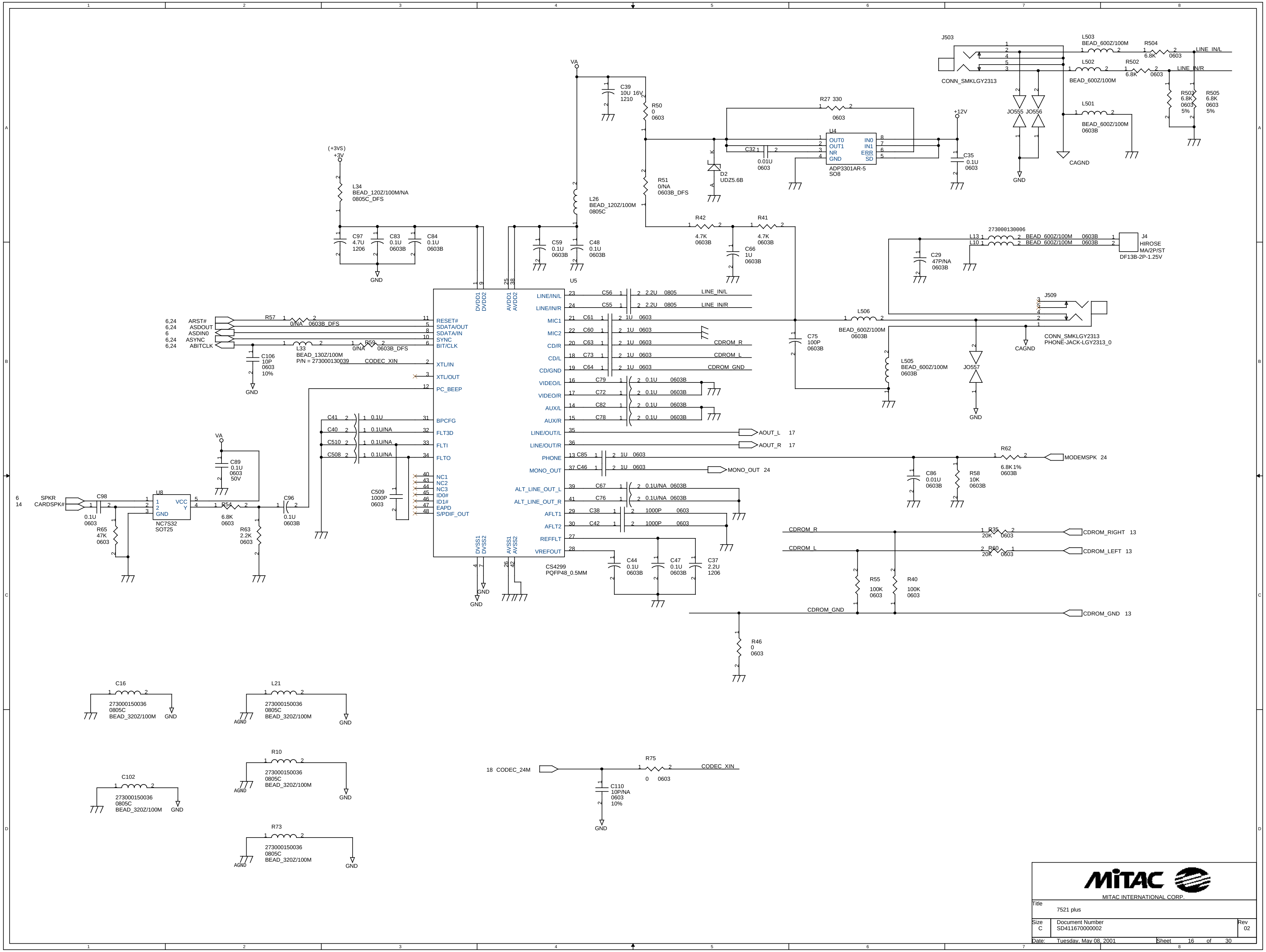
MITAC INTERNATIONAL CORP.

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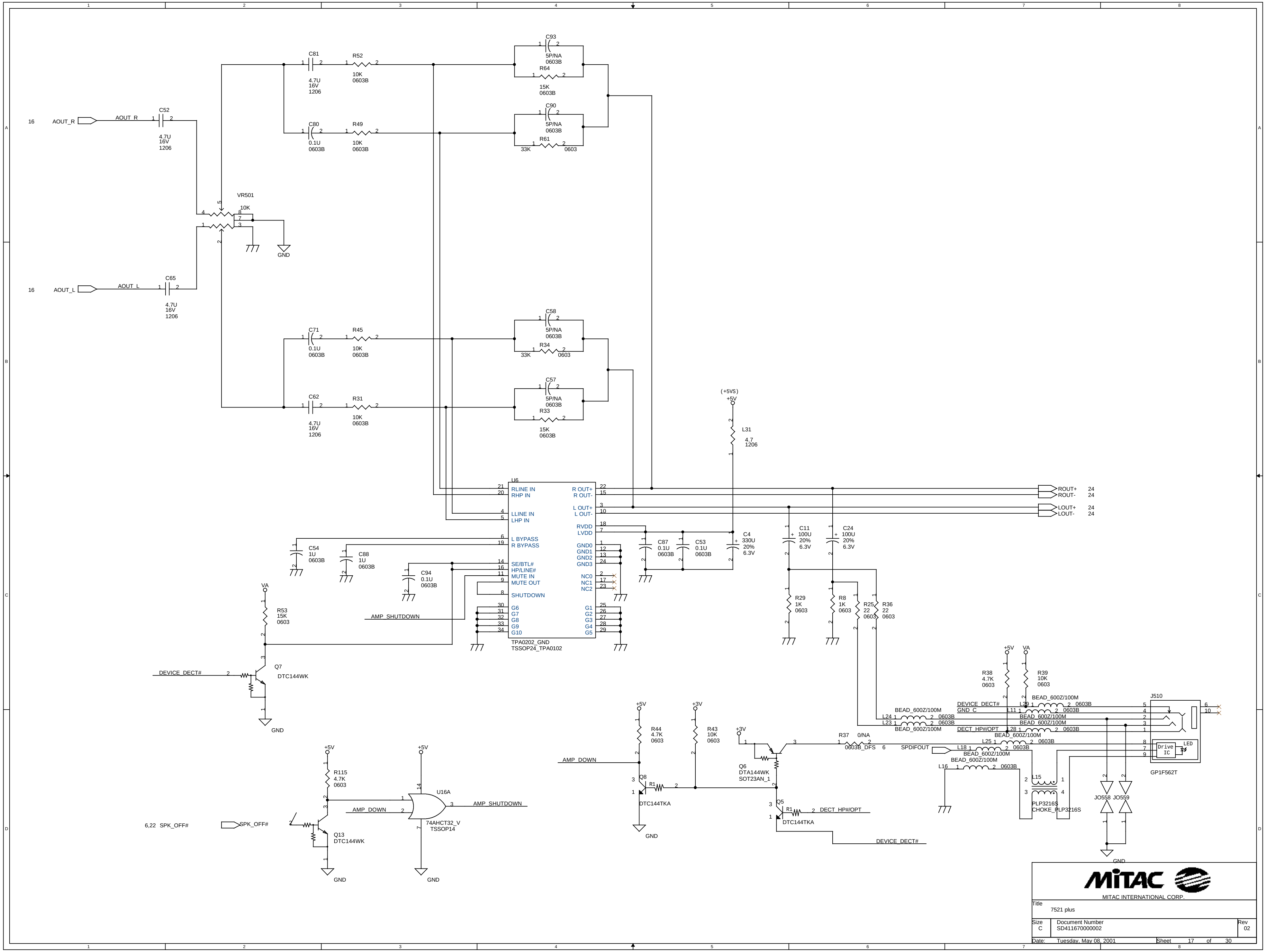


MITAC INTERNATIONAL CORP.

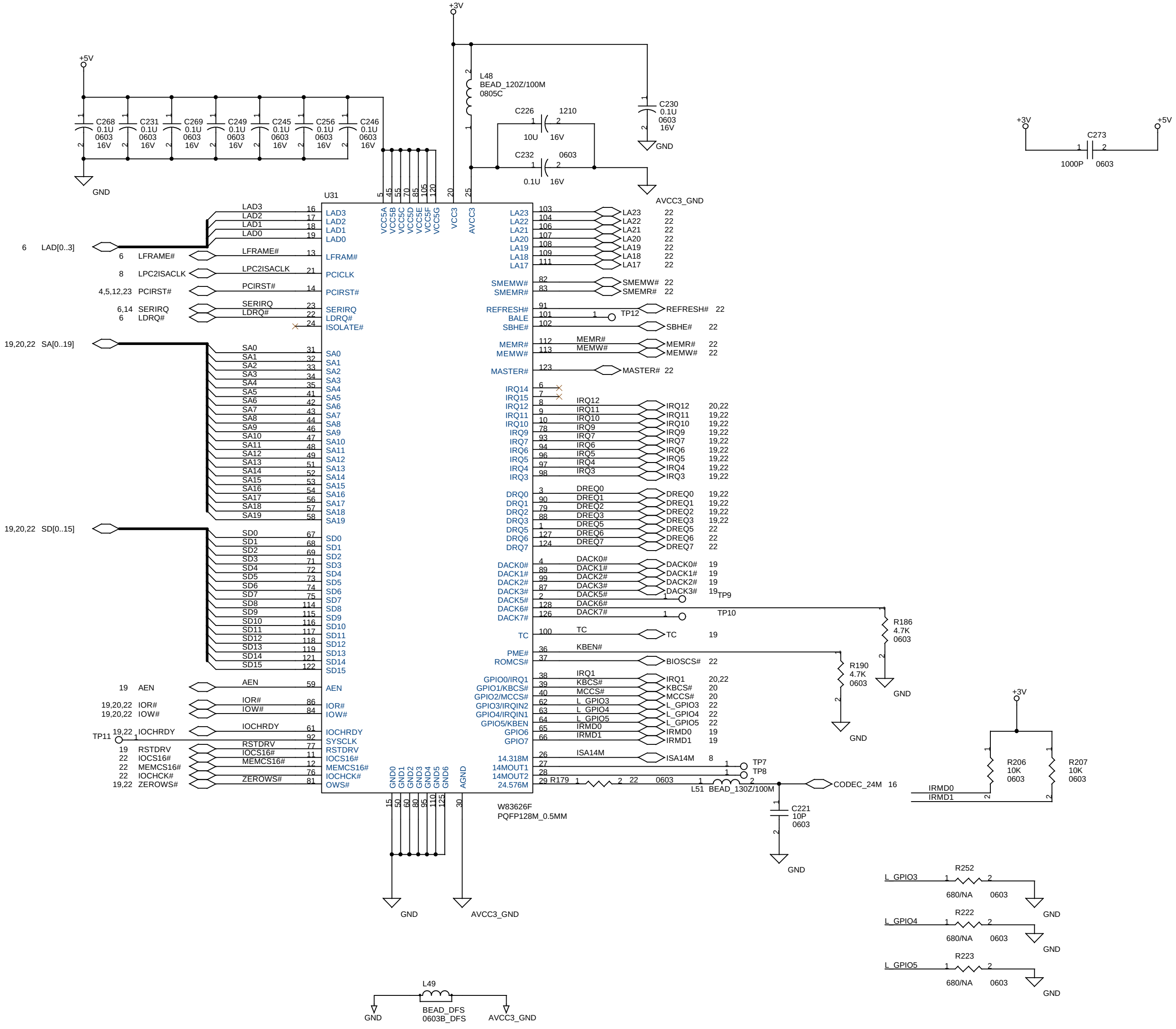
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J503
CONN_SMKLGY2313
L503
BEAD_600Z/100M
R504
6.8K
0603
LINE_IN/L
L502
R502
LINE_IN/R
R503
R505
6.8K
0603
5%
L501
BEAD_600Z/100M
0603B
JO555
JO556
GND
CAGND
VA
C39
10U 16V
1210
R50
0
0603
R27 330
0603
U4
OUT0
OUT1
NR
GND
IN0
IN1
ERR
SD
ADP3301AR-5
SO8
+12V
C35
0.1U
0603
C32
0.01U
0603
D2
UDZ5.6B
R51
0/NA
0603B_DFS
(+3VS)
+3V
L34
BEAD_120Z/100M/NA
0805C_DFS
L26
BEAD_120Z/100M
0805C
R42
4.7K
0603B
R41
4.7K
0603B
C66
1U
0603B
C97
4.7U
1206
C83
0.1U
0603B
C84
0.1U
0603B
C59
0.1U
0603B
C48
0.1U
0603B
273000130006
L13
L10
BEAD_600Z/100M
0603B
J4
HIROSE
MA/2P/ST
DF13B-2P-1.25V
C29
47P/NA
0603B
U5
DVDD1
DVDD2
AVDD1
AVDD2
LINE/IN/L
LINE/IN/R
MIC1
MIC2
CD/R
CD/L
CD/GND
VIDEO/L
VIDEO/R
AUX/L
AUX/R
LINE/OUT/L
LINE/OUT/R
PHONE
MONO_OUT
ALT_LINE_OUT_L
ALT_LINE_OUT_R
AFLT1
AFLT2
REFFLT
VREFOUT
RESET#
SDATA/OUT
SDATA/IN
SYNC
BIT/CLK
XTL/IN
XTL/OUT
PC_BEEP
BPCFG
FLT3D
FLTI
FLTO
NC1
NC2
NC3
ID0#
ID1#
EAPD
S/PDIF_OUT
DVSS1
DVSS2
AVSS1
AVSS2
CS4299
PQFP48_0.5MM
C56
C55
2.2U
0805
LINE_IN/L
LINE_IN/R
C61
C60
C63
C73
C64
1U
0603
CDROM_R
CDROM_L
CDROM_GND
C79
C72
C82
C78
0.1U
0603B
J509
L506
BEAD_600Z/100M
0603B
C75
100P
0603B
L505
BEAD_600Z/100M
0603B
CONN_SMKLGY2313
PHONE-JACK-LGY2313_0
JO557
6,24
6,24
6
6,24
6,24
ARST#
ASDOUT
ASDIN0
ASYNC
ABITCLK
R57
0/NA
0603B_DFS
L33
BEAD_130Z/100M
P/N = 273000130039
R59
0/NA
0603B_DFS
CODEC_XIN
C106
10P
0603
10%
C41
C40
C510
C508
0.1U
0.1U/NA
C509
1000P
0603
AOUT_L 17
AOUT_R 17
C85
C46
MONO_OUT 24
R62
6.8K 1%
0603B
MODEMSPK 24
C86
0.01U
0603B
R58
10K
0603B
C67
C76
0.1U/NA
0603B
C38
C42
1000P
0603
C44
0.1U
0603B
C47
0.1U
0603B
C37
2.2U
1206
R35
20K
0603
R60
20K
0603
CDROM_RIGHT 13
CDROM_LEFT 13
R55
100K
0603
R40
100K
0603
CDROM_GND 13
R46
0
0603
C89
0.1U
0603
50V
6
14
SPKR
CARDSPK#
C98
0.1U
0603
U8
VCC
Y
GND
NC7S32
SOT25
R54
6.8K
0603
R65
47K
0603
R63
2.2K
0603
C96
0.1U
0603B
C16
273000150036
0805C
BEAD_320Z/100M
L21
AGND
R10
C102
R73
18 CODEC_24M
R75
0 0603
C110
10P/NA
0603
10%
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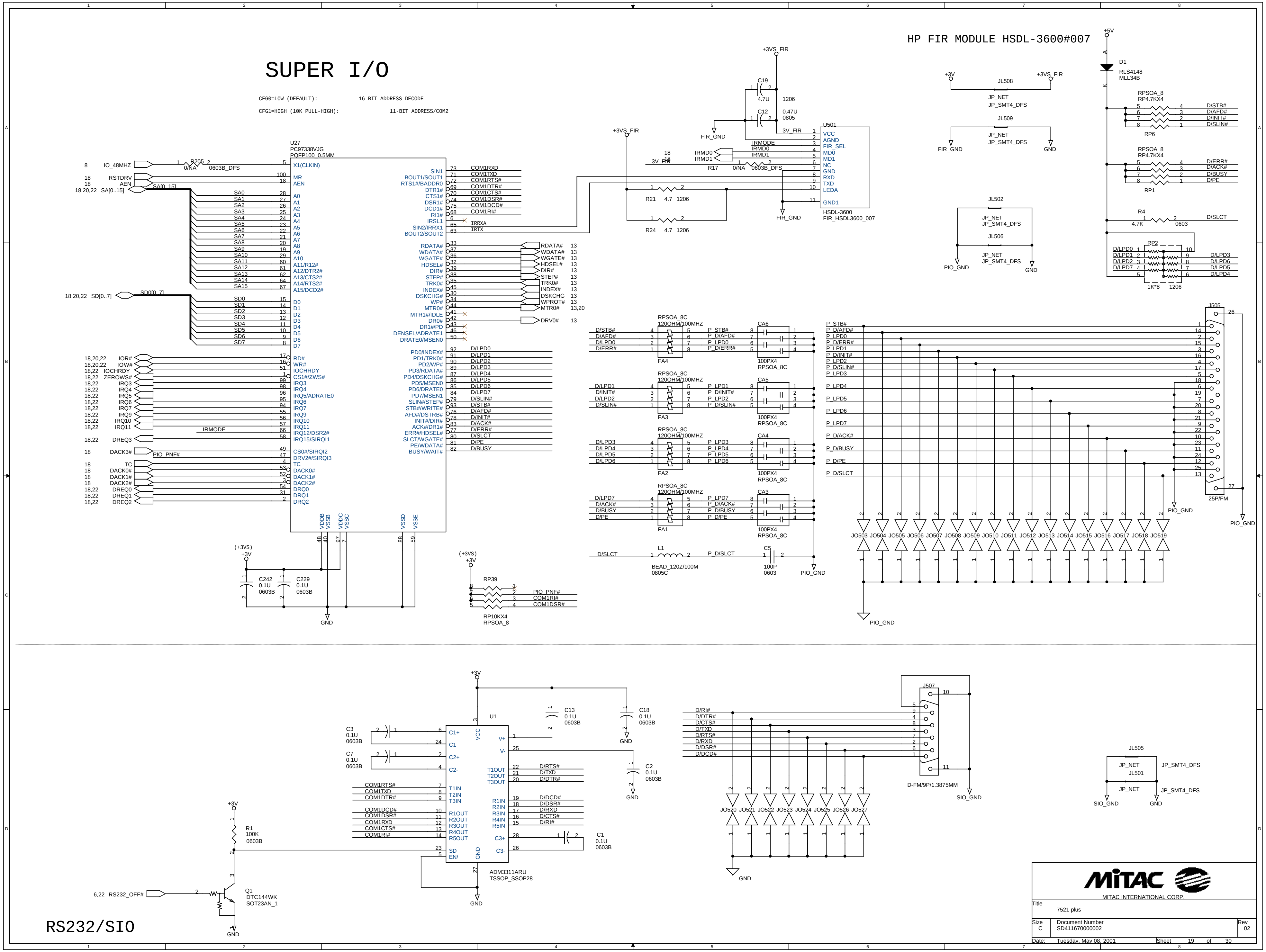


16 AOUT_R
AOUT_R
C52 4.7U 16V 1206
16 AOUT_L
AOUT_L
C65 4.7U 16V 1206
VR501 10K
GND
C81 4.7U 16V 1206
R52 10K 0603B
C80 0.1U 0603B
R49 10K 0603B
C93 5P/NA 0603B
R64 15K 0603B
C90 5P/NA 0603B
R61 33K 0603
C71 0.1U 0603B
R45 10K 0603B
C62 4.7U 16V 1206
R31 10K 0603B
C58 5P/NA 0603B
R34 33K 0603
C57 5P/NA 0603B
R33 15K 0603B
(+5VS) +5V
L31 4.7 1206
U6
RLINE IN
RHP IN
LLINE IN
LHP IN
L BYPASS
R BYPASS
SE/BTL#
HP/LINE#
MUTE IN
MUTE OUT
SHUTDOWN
G6 G7 G8 G9 G10
R OUT+
R OUT-
L OUT+
L OUT-
RVDD
LVDD
GND0 GND1 GND2 GND3
NC0 NC1 NC2
G1 G2 G3 G4 G5
TPA0202_GND
TSSOP24_TPA0102
ROUT+ 24
ROUT- 24
LOUT+ 24
LOUT- 24
C54 1U 0603B
C88 1U 0603B
C94 0.1U 0603B
C87 0.1U 0603B
C53 0.1U 0603B
C4 330U 20% 6.3V
C11 100U 20% 6.3V
C24 100U 20% 6.3V
R29 1K 0603
R8 1K 0603
R25 22 0603
R36 22 0603
VA
R53 15K 0603
AMP_SHUTDOWN
DEVICE_DECT#
Q7 DTC144WK
GND
+5V
R38 4.7K 0603
VA
R39 10K 0603
J510
BEAD_600Z/100M
DEVICE_DECT#
GND_C
L29 0603B
L11 0603B
L24 0603B
L23 0603B
DECT_HP#/OPT
L28 0603B
L25 0603B
L18 0603B
L16 0603B
SPDIFOUT
Drive IC
LED
GP1F562T
L15
PLP3216S
CHOKE_PLP3216S
JO558 JO559
GND
+5V
R44 4.7K 0603
+3V
R43 10K 0603
+3V
R37 0/NA 0603B_DFS 6
AMP_DOWN
Q8 DTC144TKA
Q6 DTA144WK SOT23AN_1
Q5 DTC144TKA
DECT_HP#/OPT
DEVICE_DECT#
GND
+5V
R115 4.7K 0603
+5V
U16A
AMP_DOWN
AMP_SHUTDOWN
74AHCT32_V TSSOP14
6,22 SPK_OFF#
SPK_OFF#
Q13 DTC144WK
GND
GND
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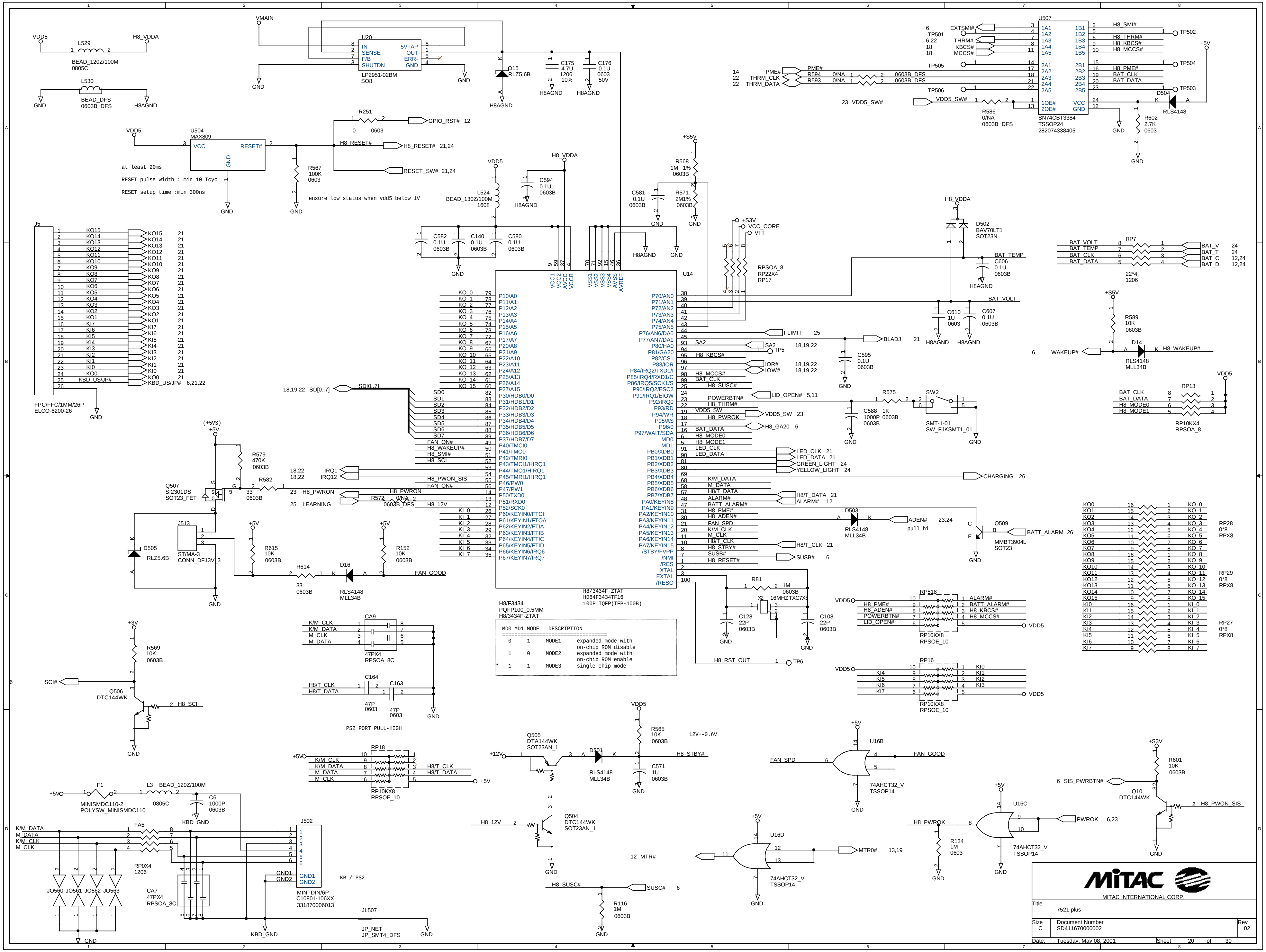


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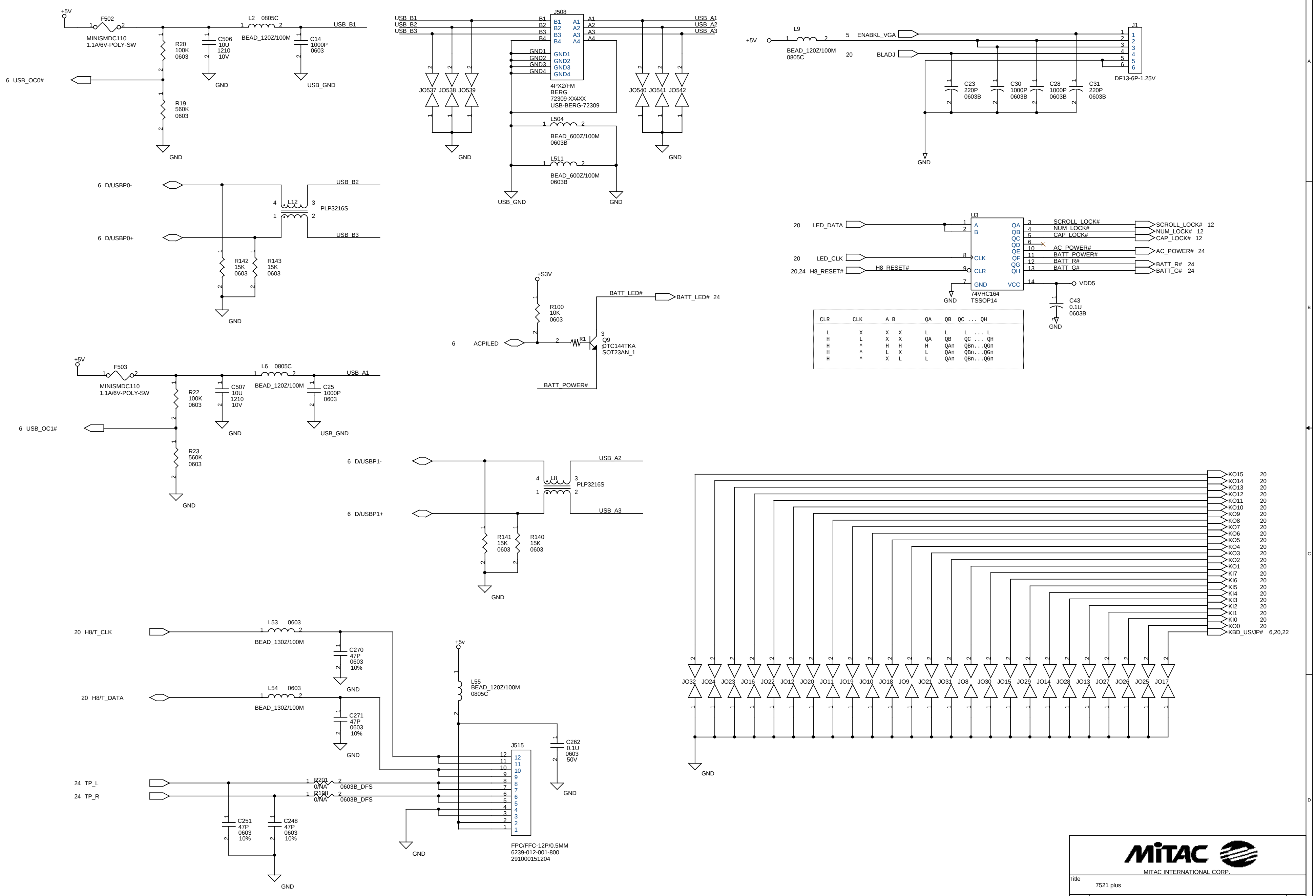


SUPER I/O
CFG0=LOW (DEFAULT): 16 BIT ADDRESS DECODE
CFG1=HIGH (10K PULL-HIGH): 11-BIT ADDRESS/COM2
U27
PC97338VJG
PQFP100_0.5MM
HP FIR MODULE HSDL-3600#007
U501
HSDL-3600
FIR_HSDL3600_007
J505
25P/FM
RS232/SIO
U1
ADM3311ARU
TSSOP_SSOP28
J507
D-FM/9P/1.3875MM
Q1
DTC144WK
SOT23AN_1
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U14
H8/3434F-ZTAT
HD64F3434TF16
100P TQFP(TFP-100B)
H8/F3434
PQFP100_0.5MM
H8/3434F-ZTAT
MD0 MD1 MODE DESCRIPTION
0 1 MODE1 expanded mode with on-chip ROM disable
1 0 MODE2 expanded mode with on-chip ROM enable
* 1 1 MODE3 single-chip mode
U504
MAX809
at least 20ms
RESET pulse width : min 10 Tcyc
RESET setup time :min 300ns
ensure low status when vdd5 below 1V
U20
LP2951-02BM
SO8
U507
SN74CBT3384
TSSOP24
282074338405
J5
FPC/FFC/1MM/26P
ELCO-6200-26
PS2 PORT PULL-HIGH
J502
MINI-DIN/6P
C10801-106XX
331870006013
KB / PS2
U16B
74AHCT32_V
TSSOP14
U16C
74AHCT32_V
TSSOP14
U16D
74AHCT32_V
TSSOP14
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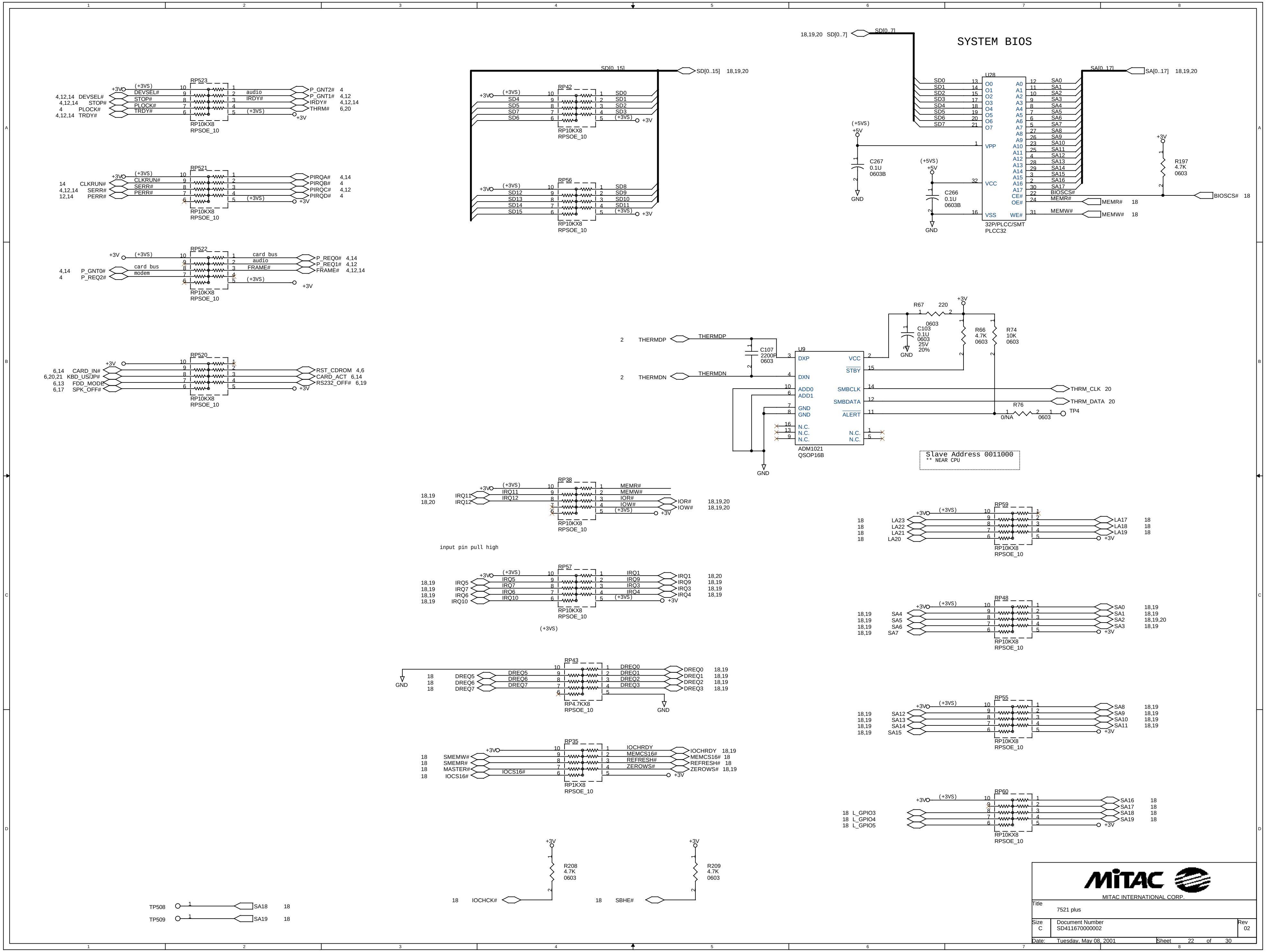
USB CONNECTOR



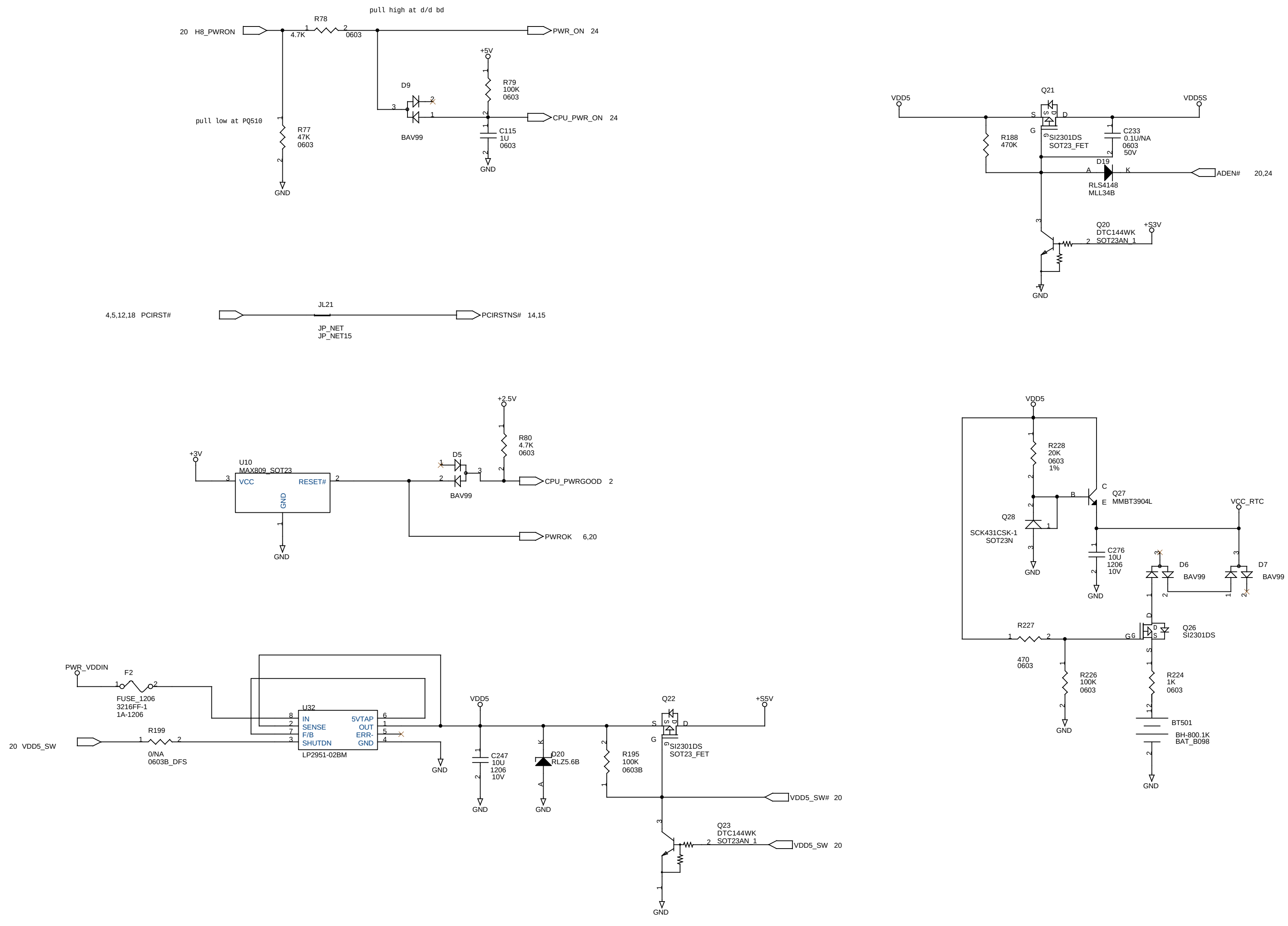
CLR	CLK	A	B	QA	QB	QC ... QH
L	X	X	X	L	L	L ... L
H	L	X	X	QA	QB	QC ... QH
H	^	H	H	H	QAn	QBn...QGn
H	^	L	X	L	QAn	QBn...QGn
H	^	X	L	L	QAn	QBn...QGn

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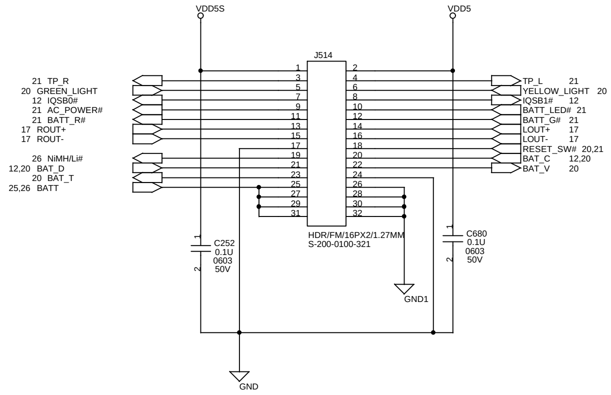
SYSTEM BIOS
SD[0..7]
SD[0..15]
SA[0..17]
U28
32P/PLCC/SMT
PLCC32
VPP
VCC
VSS
CE#
OE#
WE#
BIOSCS#
MEMR#
MEMW#
C267
0.1U
0603B
C266
0.1U
0603B
R197
4.7K
0603
RP523
RP521
RP522
RP520
RP42
RP56
RP10KX8
RPSOE_10
P_GNT2#
P_GNT1#
IRDY#
THRM#
DEVSEL#
STOP#
PLOCK#
TRDY#
CLKRUN#
SERR#
PERR#
PIRQA#
PIRQB#
PIRQC#
PIRQD#
P_REQ0#
P_REQ1#
FRAME#
P_GNT0#
P_REQ2#
card bus
audio
modem
CARD_IN#
KBD_US/JP#
FDD_MODE
SPK_OFF#
RST_CDROM
CARD_ACT
RS232_OFF#
U9
ADM1021
QSOP16B
THERMDP
THERMDN
C107
2200P
0603
R67
220
0603
C103
0.1U
0603
25V
20%
R66
4.7K
0603
R74
10K
0603
R76
0/NA
0603
TP4
DXP
DXN
ADD0
ADD1
GND
N.C.
STBY
SMBCLK
SMBDATA
ALERT
THRM_CLK
THRM_DATA
Slave Address 0011000
** NEAR CPU
RP38
RP57
RP43
RP4.7KX8
RP35
RP1KX8
RP59
RP48
RP55
RP60
input pin pull high
IRQ11
IRQ12
IOR#
IOW#
IRQ1
IRQ9
IRQ3
IRQ4
IRQ5
IRQ7
IRQ6
IRQ10
DREQ0
DREQ1
DREQ2
DREQ3
DREQ5
DREQ6
DREQ7
IOCHRDY
MEMCS16#
REFRESH#
ZEROWS#
SMEMW#
SMEMR#
MASTER#
IOCS16#
LA17
LA18
LA19
LA20
LA21
LA22
LA23
L_GPIO3
L_GPIO4
L_GPIO5
R208
4.7K
0603
R209
4.7K
0603
IOCHCK#
SBHE#
TP508
TP509
SA18
SA19
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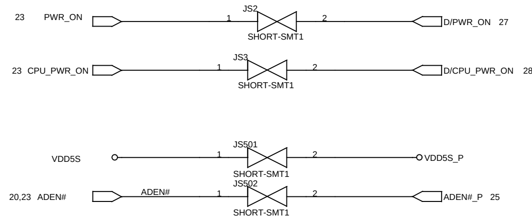
SUSTAT1#	SUSTAT2#	SUSA#	SUSB#	SUSC#		VDD5	+5V51	VDD3	+12V	+5V	+5VS	+3V	+3VS	CPU_IO	CPU_CORE
0	0	0	0	0	FULL ON	0	0	0	0	0	0	0	0	0	0
X	X	X	0	0	POS	0	0	0	0	0	0	0	0	0	0
X	X	X	X	0	STR	0	0	0	0	0	X	0	X	X	X
X	X	X	X	X	STD(SOFT OFF) (ACIN OR BATTERY IN)	0	0 / X ADIN / BAT	0	X	X	X	X	X	X	X
X	X	X	X	X	MECH OFF (NO ACIN & NO BATT)	X	X	X	X	X	X	X	X	X	X

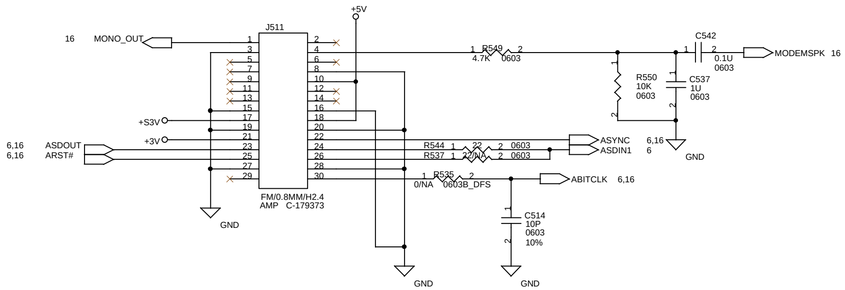
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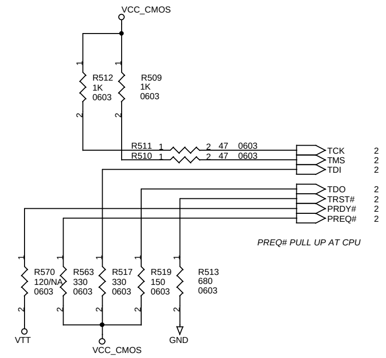
Title	7521 plus	
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Charger board connector

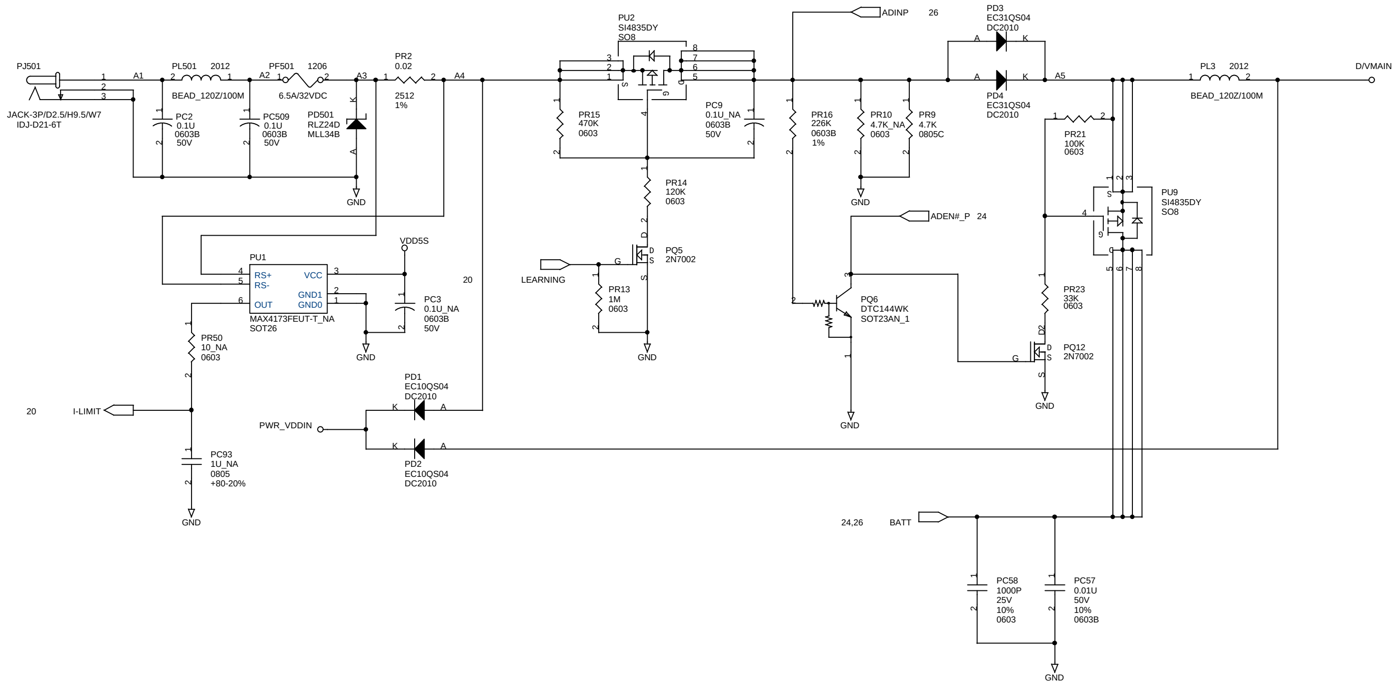






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Title	7521 plus		
Size C	Document Number SD411670000002		Rev 02
Date: Tuesday, May 08, 2001	Sheet 24 of 30		

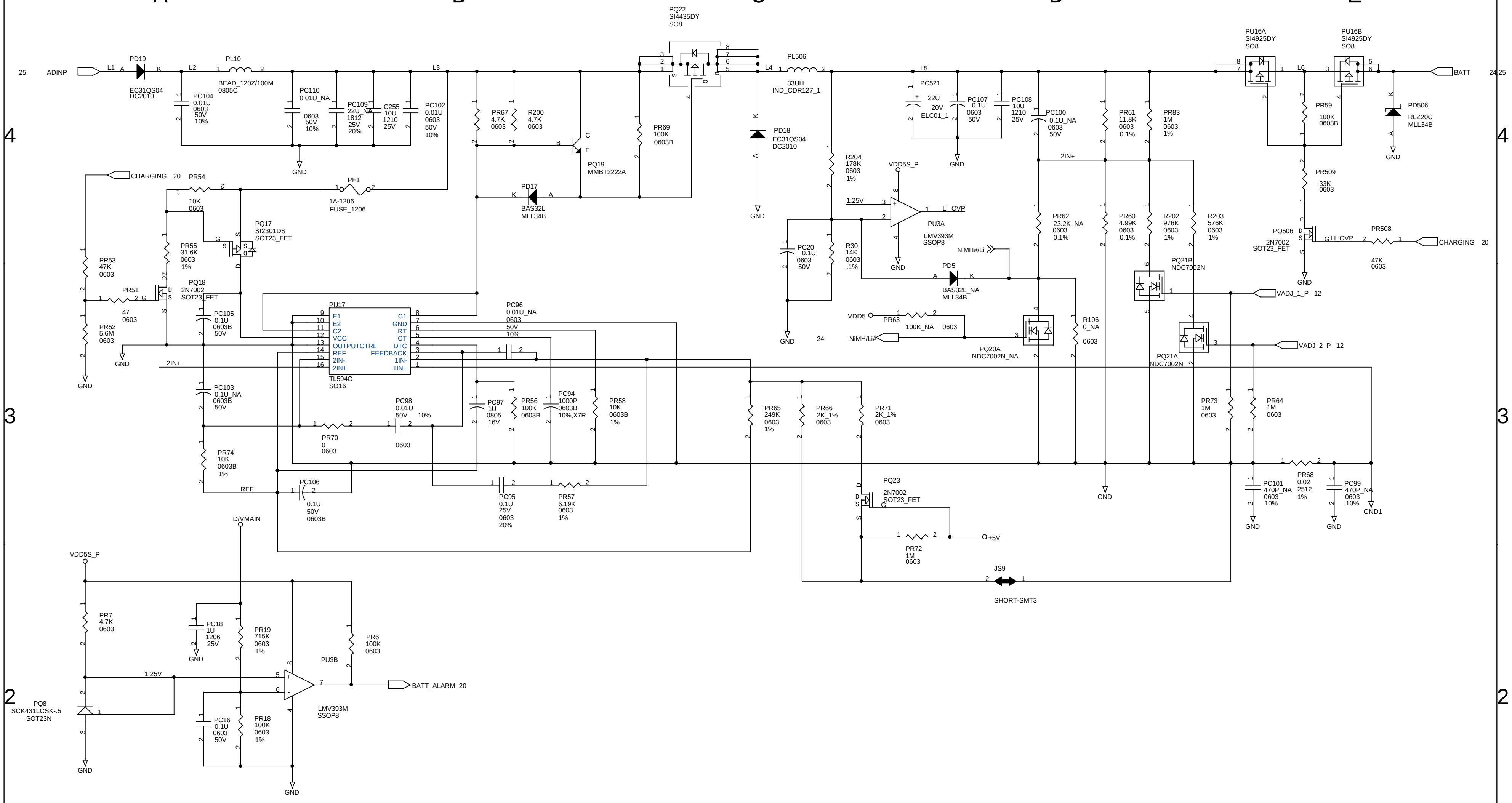


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Title: **7521 plus_ADINP & DISCHARGE**

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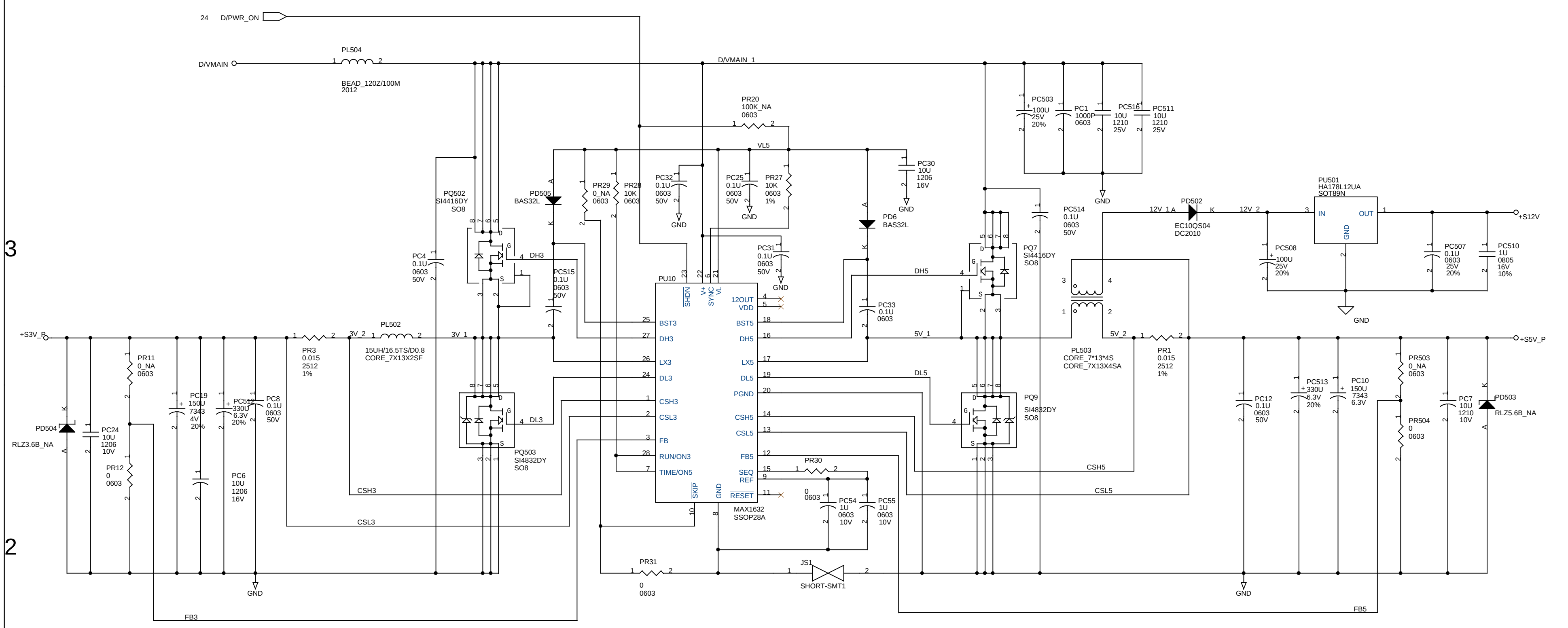
	VADJ_2_P	VADJ_1_P
16.60V	0	0
16.65V	0	1
16.70V	1	0
16.75V	1	1

MiTAC

Title: 7521 plus_CHARGER

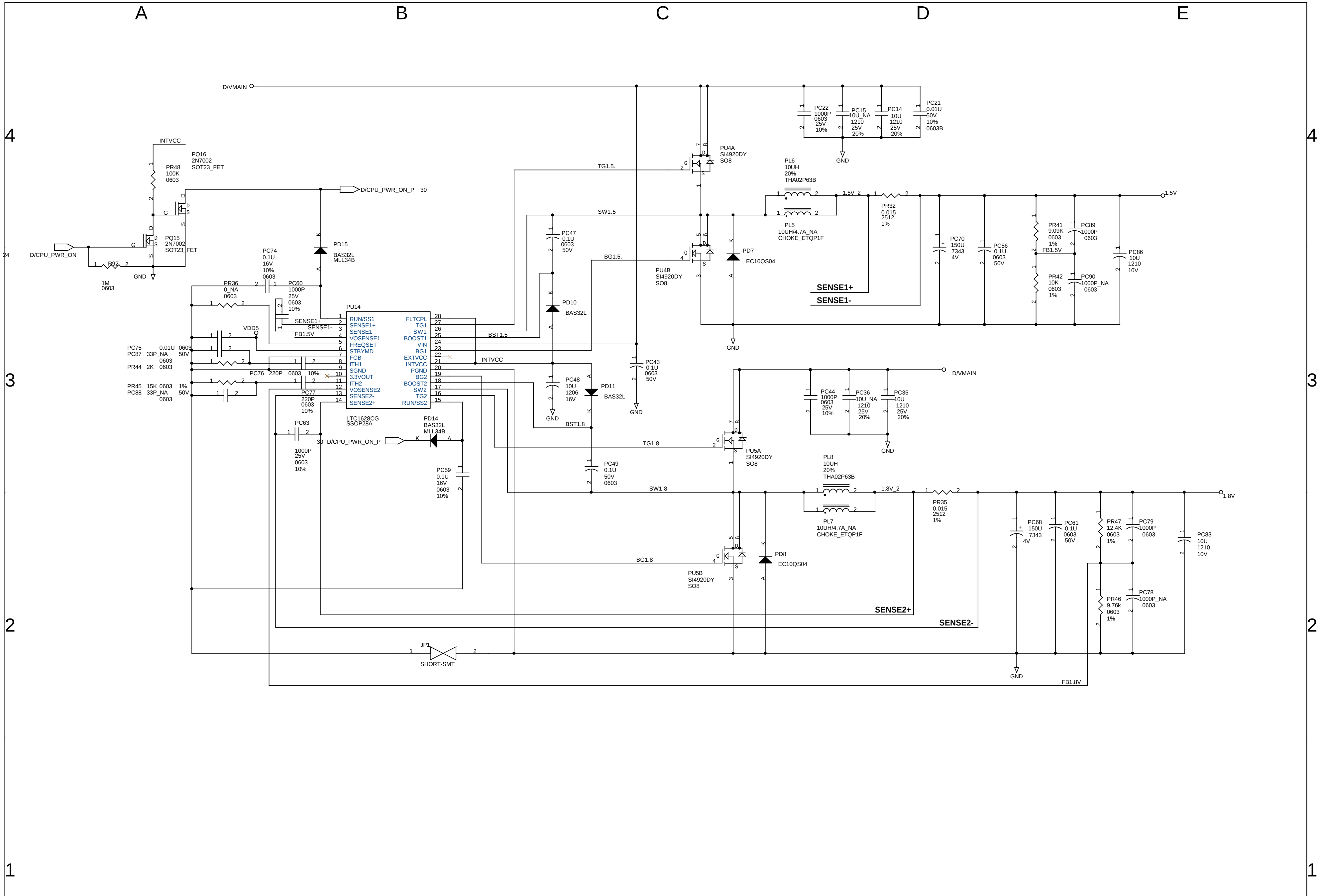
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7521 plus S5V S3V S12V

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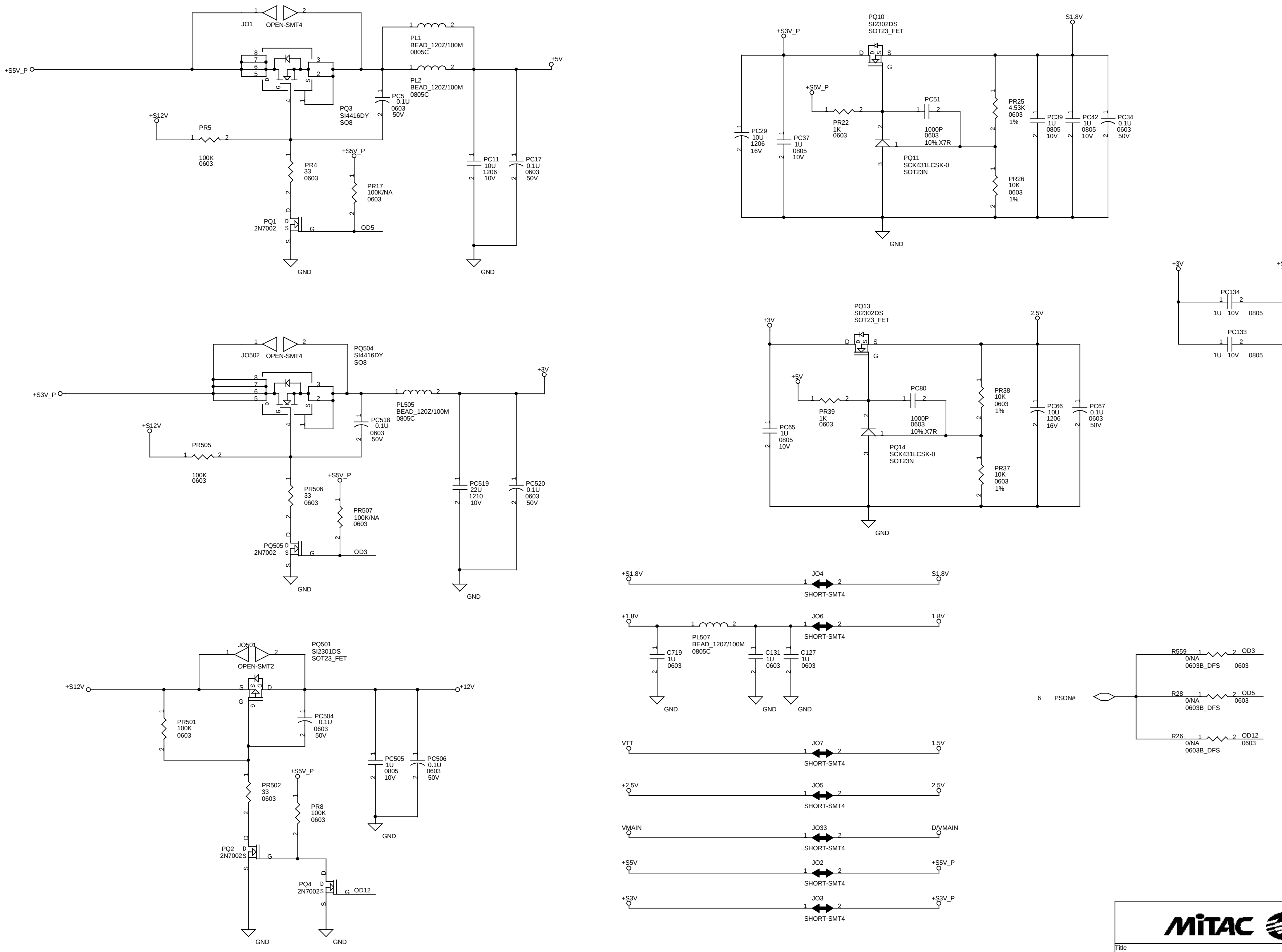


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Title: 7521 plus 1.5V/1.8V

Size	Document Number	Rev
C	SD411670000002	02

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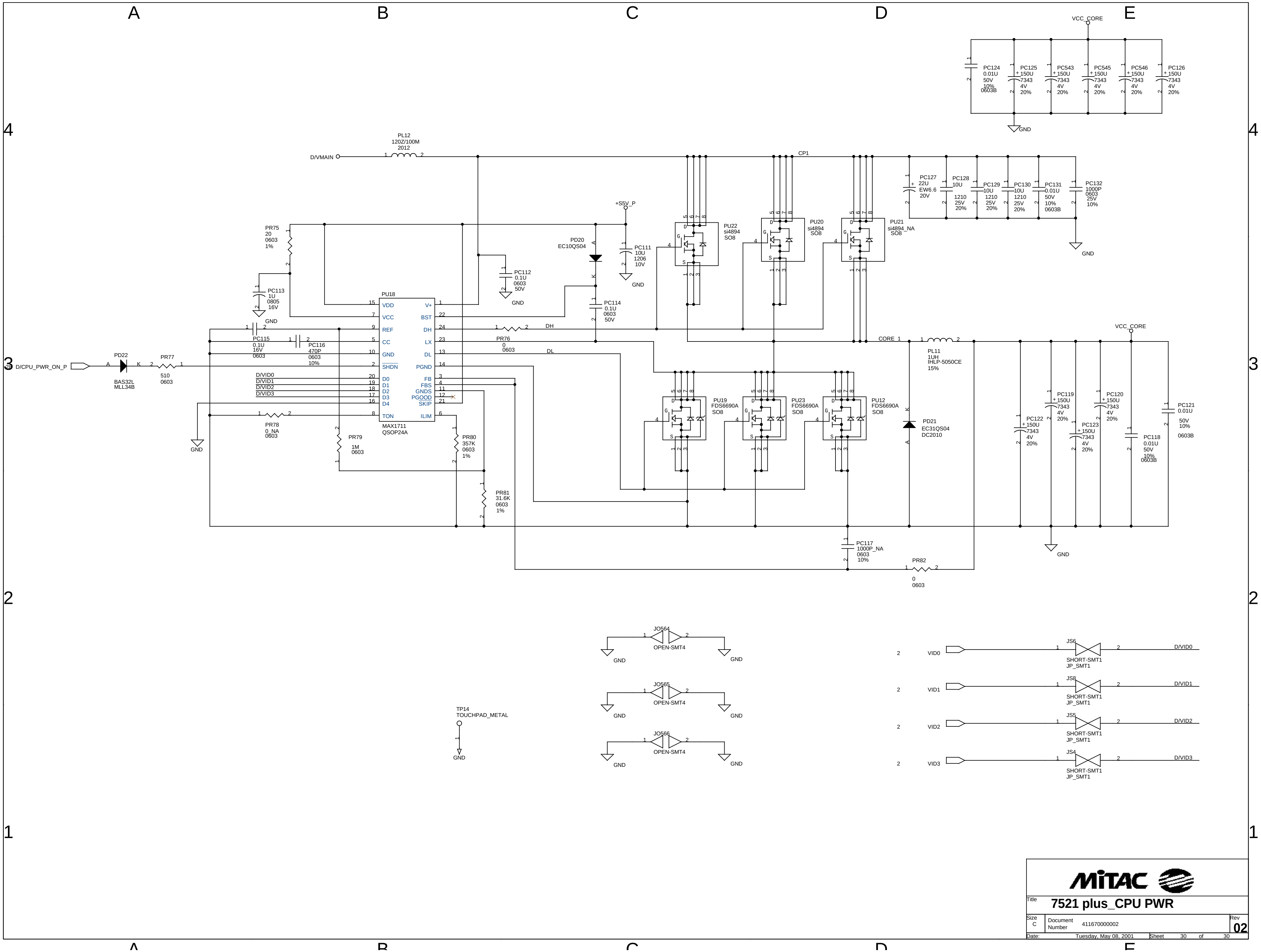


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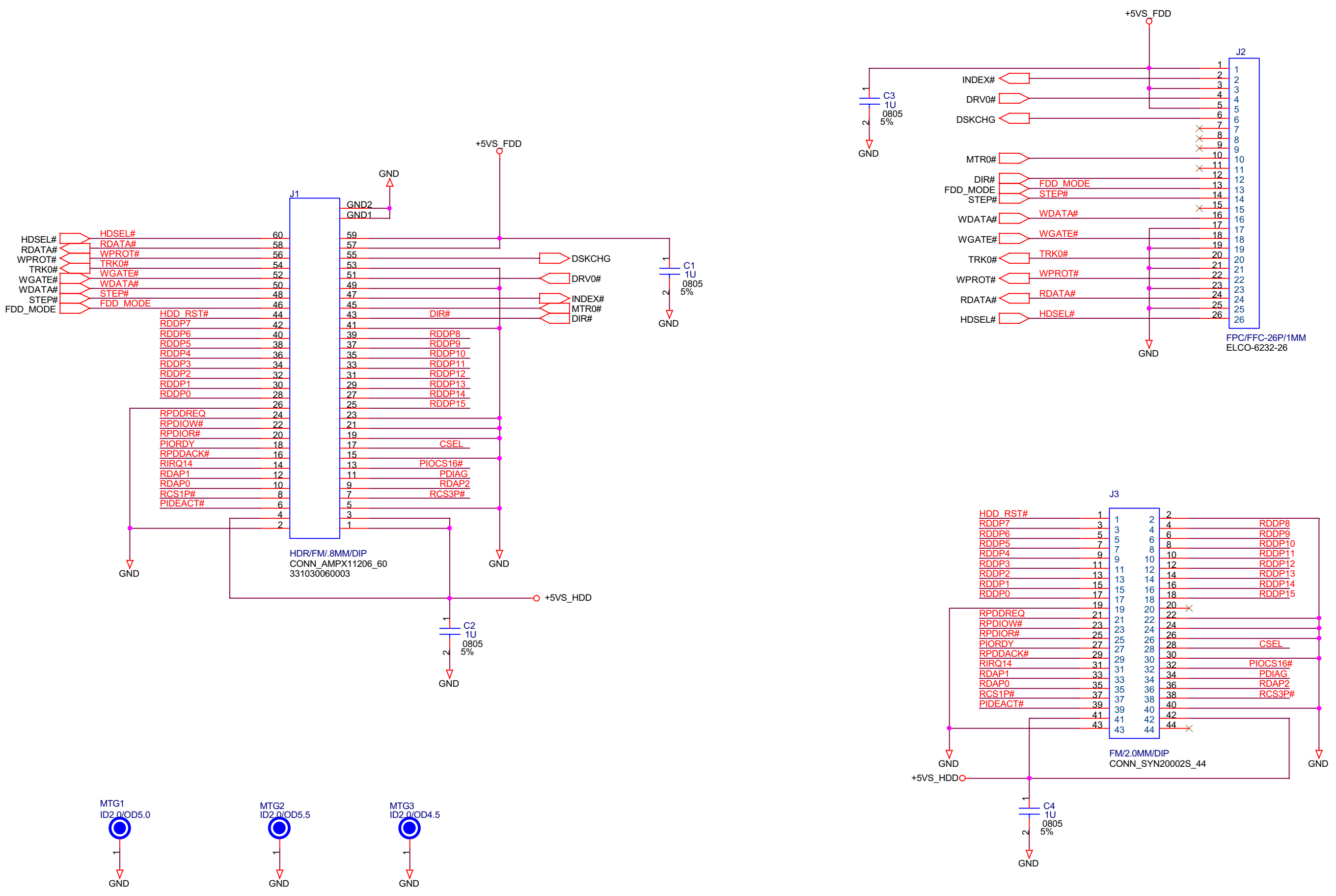
Title: 7521 plus_+5V_+3V_+12V_S1.8V_2.5V

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VCC_CORE
PC124 0.01U 50V 10% 0603B
PC125 150U 7343 4V 20%
PC543 150U 7343 4V 20%
PC545 150U 7343 4V 20%
PC546 150U 7343 4V 20%
PC126 150U 7343 4V 20%
GND
PL12 120Z/100M 2012
D/VMAIN
CP1
PC127 22U EW6.6 20V
PC128 10U 1210 25V 20%
PC129 10U 1210 25V 20%
PC130 10U 1210 25V 20%
PC131 0.01U 50V 10% 0603B
PC132 1000P 0603 25V 10%
+S5V_P
PD20 EC10QS04
PC111 10U 1206 10V
PC112 0.1U 0603 50V
PC113 1U 0805 16V
PC114 0.1U 0603 50V
PR75 20 0603 1%
PU22 si4894 SO8
PU20 si4894 SO8
PU21 si4894_NA SO8
PU18
MAX1711 QSOP24A
VDD VCC REF CC GND SHDN D0 D1 D2 D3 D4 TON
V+ BST DH LX DL PGND FB FBS GNDS PGOOD SKIP ILIM
PC115 0.1U 16V 0603
PC116 470P 0603 10%
PR76 0 0603
DH
DL
CORE_1
PL11 1UH IHLP-5050CE 15%
D/CPU_PWR_ON_P
PD22 BAS32L MLL34B
PR77 510 0603
D/VID0
D/VID1
D/VID2
D/VID3
PR78 0_NA 0603
PR79 1M 0603
PR80 357K 0603 1%
PR81 31.6K 0603 1%
PU19 FDS6690A SO8
PU23 FDS6690A SO8
PU12 FDS6690A SO8
PD21 EC31QS04 DC2010
PC122 150U 7343 4V 20%
PC119 150U 7343 4V 20%
PC123 150U 7343 4V 20%
PC120 150U 7343 4V 20%
PC118 0.01U 50V 10% 0603B
PC121 0.01U 50V 10% 0603B
PC117 1000P_NA 0603 10%
PR82 0 0603
JO564 OPEN-SMT4
JO565 OPEN-SMT4
JO566 OPEN-SMT4
TP14 TOUCHPAD_METAL
VID0 JS6 SHORT-SMT1 JP_SMT1 D/VID0
VID1 JS8 SHORT-SMT1 JP_SMT1 D/VID1
VID2 JS5 SHORT-SMT1 JP_SMT1 D/VID2
VID3 JS4 SHORT-SMT1 JP_SMT1 D/VID3
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Title 7521 plus_CPU PWR
Size C Document Number 411670000002 Rev 02
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7521P HDD/FDD BD

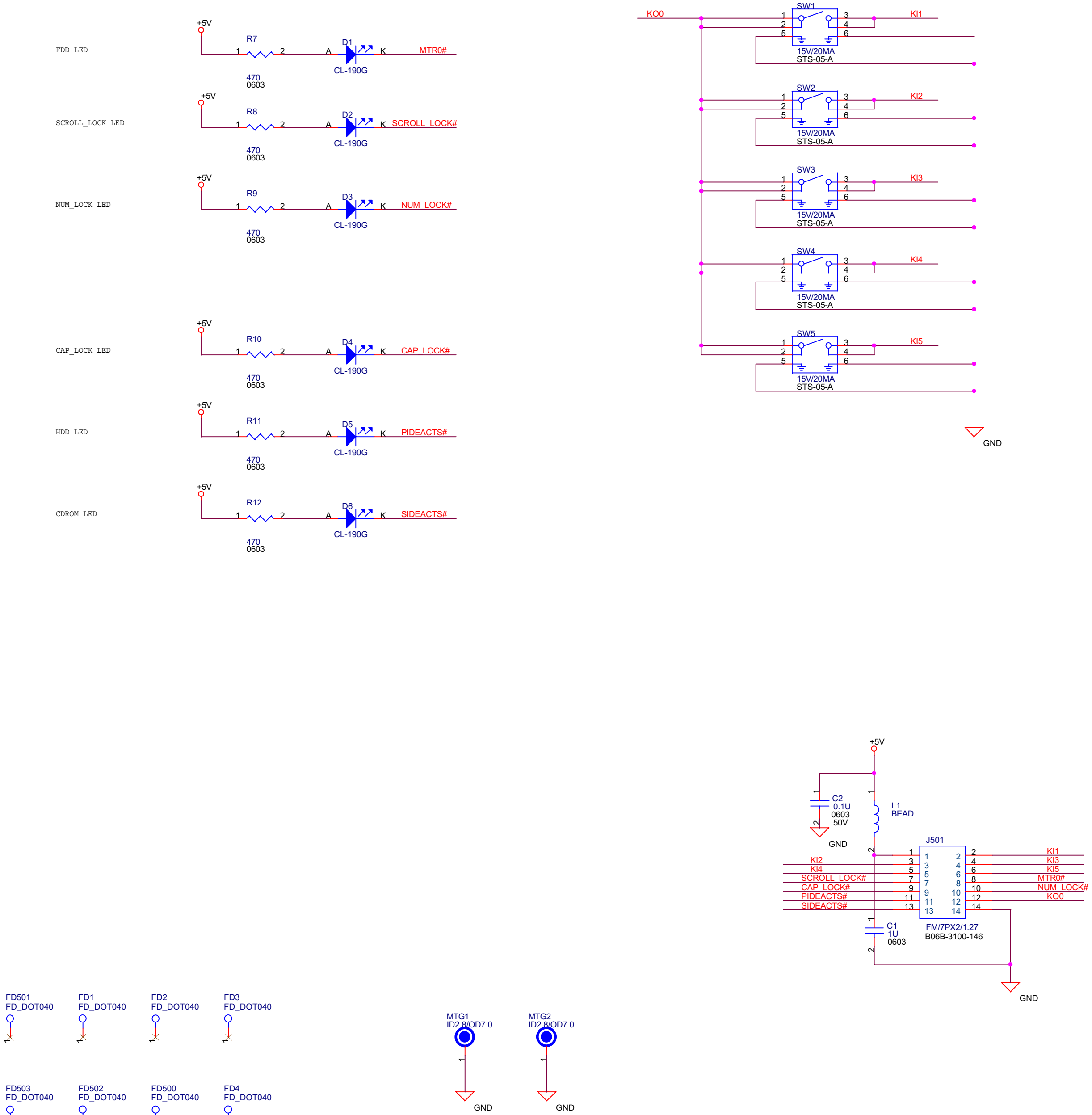


DRAWN	DESIGN	CHECK	ISSUES

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Title	7521P - FDD/HDD BD	
Size C	Document Number SD411669600014	Rev 00
Date: Tuesday, November 07, 2000	Sheet 1 of 1	

REV	DESCRIPTION OF CHANGE	ECR	DATE
R00	1.Base on RACE QSB trans bd r01.		02/15/2000



7521	7321
QSB0#	KI1
QSB1#	KI2
QSB2#	KI3
QSB3#	KI4
QSB4#	KI5
SW_GND	KO0

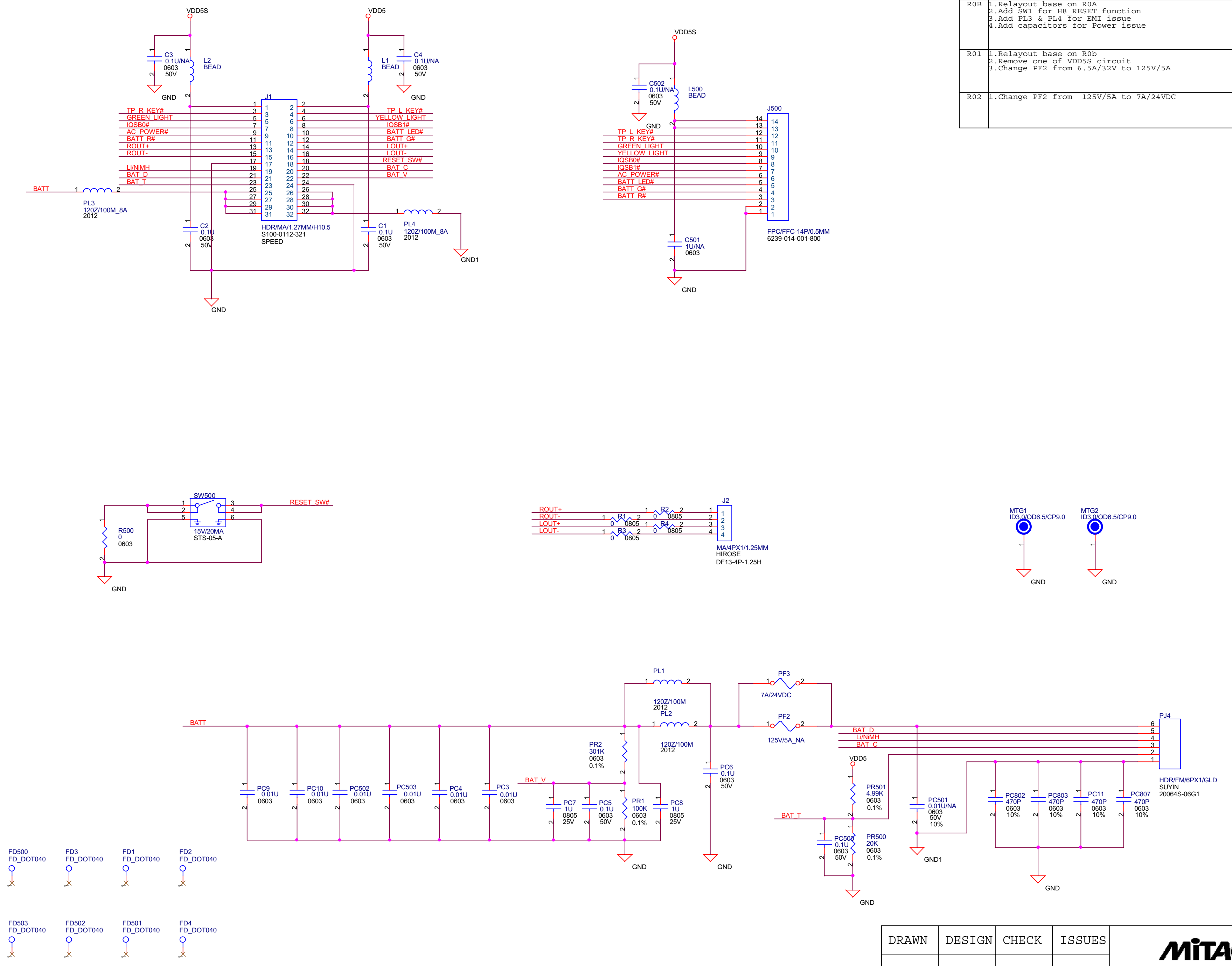
DRAWN	DESIGN	CHECK	ISSUES

MiTAC

Title: 7521P ID3 QSB BD

Size: C | Document Number: SD411670000018 | Rev: 00

Date: Friday, March 23, 2001 | Sheet 1 of 1



REV	DESCRIPTION OF CHANGE	ECR	DATE
R00			05/26/2000
R0A	1.Relayout base on R00 2.Correcting J1 shape library.		06/16/2000
R0B	1.Relayout base on R0A 2.Add SW1 for H8_RESET function 3.Add PL3 & PL4 for EMI issue 4.Add capacitors for Power issue		07/04/2000
R01	1.Relayout base on R0b 2.Remove one of VDD5S circuit 3.Change PF2 from 6.5A/32V to 125V/5A		08/15/2000
R02	1.Change PF2 from 125V/5A to 7A/24VDC		10/26/2000

DRAWN	DESIGN	CHECK	ISSUES

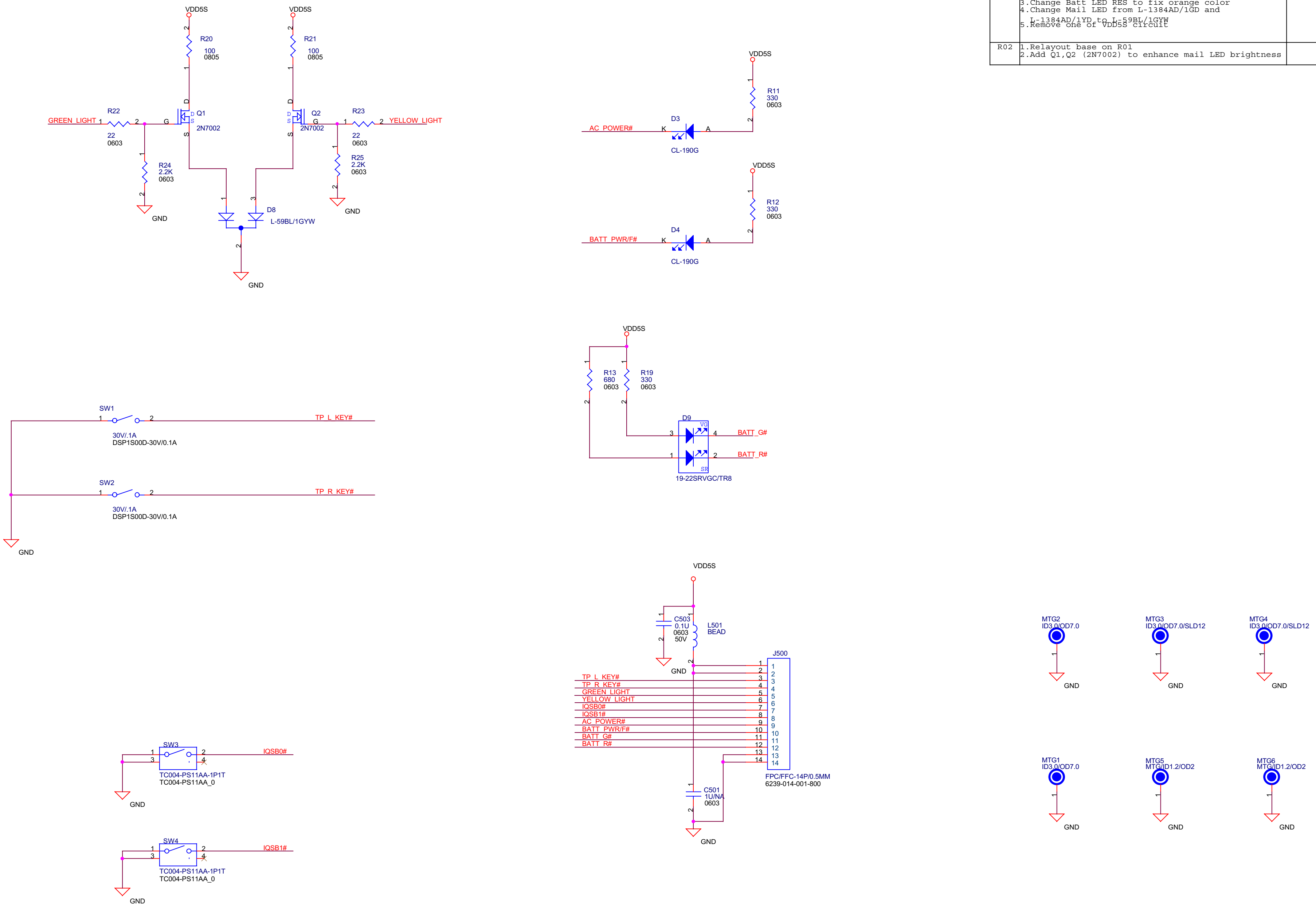
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Title: 7521P charger bd

Size: C | Document Number | Rev: 02

Date: Tuesday, May 08, 2001 | Sheet 1 of 1

REV	DESCRIPTION OF CHANGE	ECR	DATE	
R00			05/26/2000	
R0A	1.Relayout base on R00 2.Remove SW3 & SW4 pin 4 3.Remove 74164 blanking circuit 4.Reverse BATT_G# & BATT_R# pin assignment error 5.Change power source from VDD5 to VDD5S for LEDs 6.Remove the reserved circuit		07/04/2000	
R01	1.Relayout base on R0A 2.Change Batt LED from BRPG1201W to 19-22SRVGC/TR8 3.Change Batt LED RES to fix orange color 4.Change Mail LED from L-1384AD/1GD and L-1384AD/1YD to L-59BL/1GYW 5.Remove one of VDD5S circuit		08/15/2000	
R02	1.Relayout base on R01 2.Add Q1,Q2 (2N7002) to enhance mail LED brightness		09/20/2000	



DRAWN	DESIGN	CHECK	ISSUES

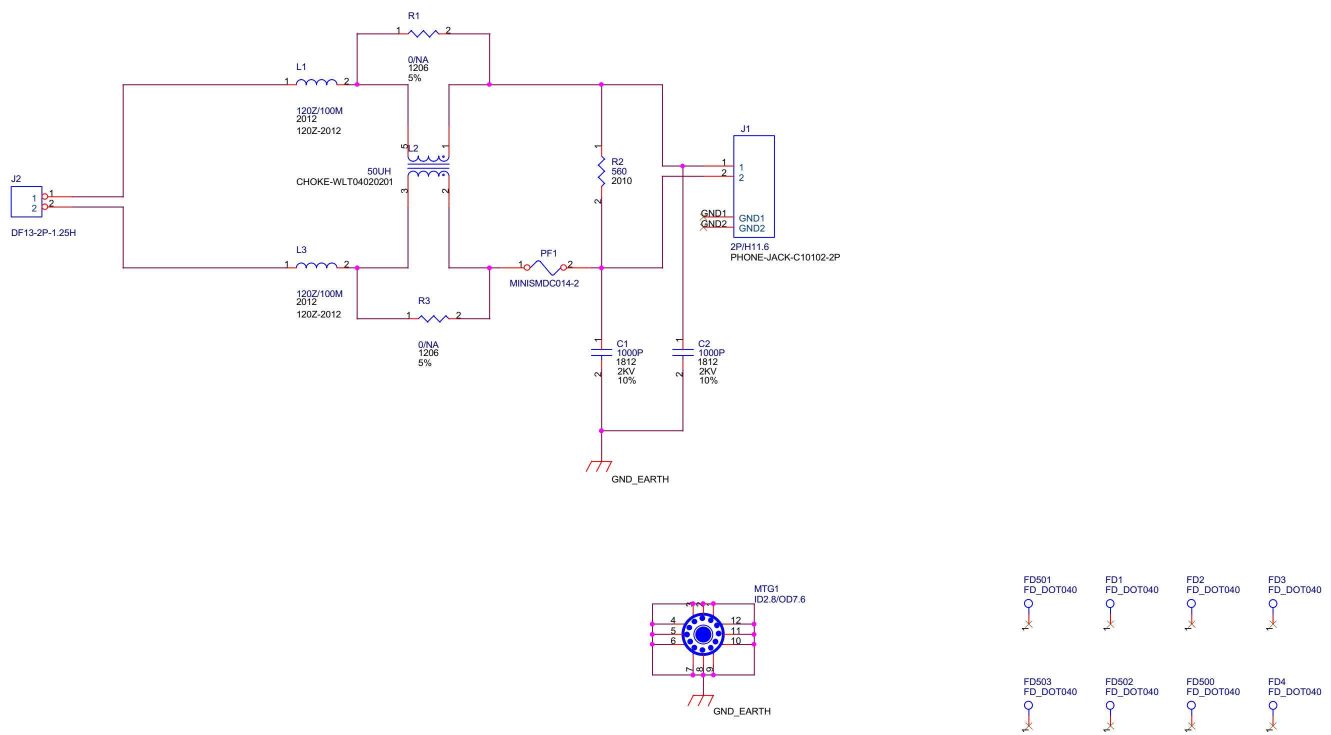
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Title: 7521P IQSB

Size	Document Number	Rev
C	SD411669600008	02

Date: Thursday, September 21, 2000 Sheet 1 of 1

REV	DESCRIPTION OF CHANGE	ECR	DATE
R00			
R0A	1.Relayout base on R00 2.Change PF1 from MINISMDC110 to MINISMD0C14-2 3.Change J2 from DF1.3B-2P-1.25v to DF1.3-2P-1.25H 4.ADD C1,C2 for MDC safety		08/15/2000
R01	1.Relayout base on R0A		09/07/2000



DRAWN	DESIGN	CHECK	ISSUES

MiTAC

Title: 7521P MDC BD

Size: C | Document Number: SD411669600006 | Rev: 01

Date: Thursday, September 07, 2000 | Sheet 1 of 1

SERVICE MANUAL & TROUBLESHOOTING GUIDE FOR 7521 Plus/N

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